SD/MMC Control Registers

SDMMC registers are accessible to ARM CPU in a 1k block.

Base address: 0xD800:A400

Offset 0x0000

SDMMC Controller

Bit	Attribute	Default	Description
4	RW		CTLR_FIFO_RESET Resets the controller FIFO buffer
2	RW		CTLR_CMD_WRITE 0: execute a read command 1: execute a write command
0	W1		CTRL_CMD_START Execute the current command

Offset 0x0001

SDMMC Command

Bit	Attribute	Default	Description
7:0	RW		CMD Command code to execute

Offset 0x0002

SDMMC Response Type

Bit	Attribute	Default	Description
7:0	RW		RSPTYPE Expected response type of command

Offset 0x0004

SDMMC Argument

Bit	Attribute	Default	Description
7:0	RW		ARG Arguments for the command

Offset 0x0008

SDMMC Bus Mode

Bit	Attribute	Default	Description
7	W1		SOFT_RESET Perform a software reset of the SDMMC controller
6	RW		SD_POWER
5	RW		SPI_CS
4	RW		SD_OFF 0: Turn off the SDMMC controller 1: Turn on the SDMMC controller
3	RW		SPI_CRC
2	RW		EIGHTBIT_MODE Set the controller to 8 bit mode (MMC)
1	RW		FOURBIT_MODE Set the controller to 4 bit mode
0	RW		SPI_MODE Set the controller to SPI mode

Offset 0x000C-0x000D

SDMMC Block Length

Bit	Attribute	Default	Description
15	RW		INT_ENABLE 1: Generate interrupts for change detect 0: No interrupts for change detect
14	RW		DATA3_CD
13	RW		GPI_CD 1: Enable CD via GPIO pin
12	RW		CD_POL_HIGH
11	RW		CRCERR_ABORT 1: Abort command on CRC error??
10:0	RW		BLK_LEN Data transfer length – 1 (Max: 2048 bytes)

Offset 0x000E-0x000F

SDMMC Block Count

Bit	Attribute	Default	Description
15:0	RW		BLK_CNT Number of blocks to transfer

Offset 0x0010-0x0013

SDMMC Response

Bit	Attribute	Default	Description
31:24	RO		RSP3
23:16	RO		RSP2
15:8	RO		RSP1
7:0	RO		RSP0 Response from the last execute command

Offset 0x0014-0x0017

SDMMC Response

Bit	Attribute	Default	Description
31:24	RO		RSP7
23:16	RO		RSP6
15:8	RO		RSP5
7:0	RO		RSP4

Offset 0x0018-0x001B

SDMMC Response

Bit	Attribute	Default	Description
31:24	RO		RSP11
23:16	RO		RSP10
15:8	RO		RSP9
7:0	RO		RSP8

Offset 0x001C-0x001F

SDMMC Response

Bit	Attribute	Default	Description
31:24	RO		RSP15
23:16	RO		RSP14
15:8	RO		RSP13
7:0	RO		RSP12

Offset 0x0020..0x0023

SDMMC Current Block Count Register

Bit	Attribute	Default	Description
31:0	RO		CBCR Current block being processed

Offset 0x0024

SDMMC Interrupt Mask #0

Bit	Attribute	Default	Description
7	RW		DI_INT_EN 1: Interrupt on device insert
6	RW		CD_INT_EN 1: Interrupt on change detect
5	RW		BLK_TRAN_DONE_INT_EN 1: Generate an interrupt when block transfer complete
4	RW		MBLK_TRAN_DONE_INT_EN 1: Generate an interrupt when multiblock transfer complete
3	RW		RH_INT_EN
2	RW		TA_INT_EN
1	RW		TE_INT_EN
0	RW		TH_INT_EN

Offset 0x0025

SDMMC Interrupt Mask #1

Bit	Attribute	Default	Description
7	RW		WRITE_CRC_ERR_INT_EN
6	RW		READ_CRC_ERR_INT_EN
5	RW		RSP_CRC_ERR_INT_EN 1: Interrupt on response CRC error
4	RW		DATA_TIMEOUT_INT_EN 1: Interrupt on data timeout
3	RW		AUTO_STOP_INT_EN
2	RW		RSP_TOUT_INT_EN 1: Interrupt on response timeout
1	RW		RSP_DONE_INT_EN 1: Interrupt on response transfer complete
0	RW		SDIO_INT_EN

Offset 0x0028

SDMMC Status Register 0

Bit	Attribute	Default	Description
7	W1C		DEVICE_INS 1: Device insertion changed
6	W1C		CARD_DETECT 1: Card detect changed
5	W1C		BLK_TRANS_DONE 1: Block transfer completed
4	W1C		MULTI_BLK_TRANS_DONE
3	W1C		CD_GPI 1: Change Detect on GPIO
2	W1C		CD_DATA3 1: Changed Detect on DATA3
1	W1C		WRITE_PROTECT 1: card is write-protected 0: card is read-write
0	W1C		TH

Offset 0x0029

SDMMC Status Register 1

Bit	Attribute	Default	Description
7	W1C		WRITE_CRC_ERR
6	W1C		READ_CRC_ERR
5	W1C		RSP_CRC_ERR 1: Response contained a CRC error
4	W1C		DATA_TIMEOUT 1: Timeout occurred during data transfer
3	W1C		AUTOSTOP_DONE
2	W1C		RSP_TIMEOUT 1: Command response timed out
1	W1C		RSP_DONE 1: Command response completed
0	W1C		SDIO_INT

Offset 0x002A

SDMMC Status Register 2

Bit	Attribute	Default	Description
7	W1C		CLK_FREEZE_EN
6	W1C		CLK_FREEZE_STS
5	W1C		RSP_BUSY 1: Command response returned busy

Offset 0x0034

SDMMC Ext Control

Bit	Attribute	Default	Description
7	RW		HS MODE 1: High speed mode 0: Low speed mode
6..3			Reserved
2	RW		0: One Bit / Four bit mode 1: Eight bit mode
1			Reserved
0	RW		AUTOSTOP 1: Enable autostop

Offset 0x003C..0x003D

SDMMC DMA Timeout

Bit	Attribute	Default	Description
15:0	RW		DMA_TIMEOUT DMA timeout value.