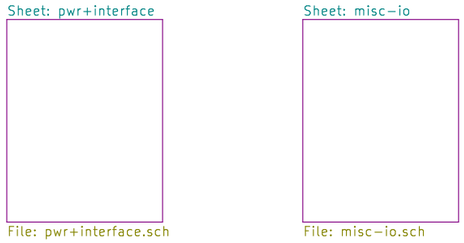
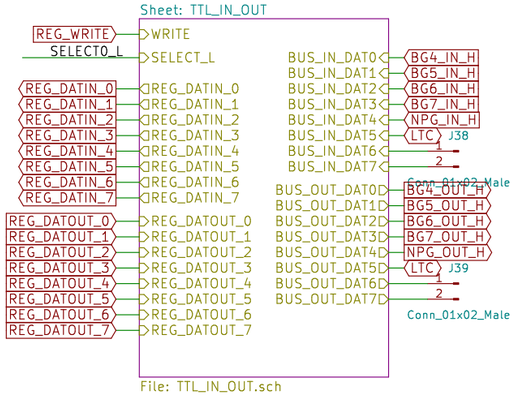
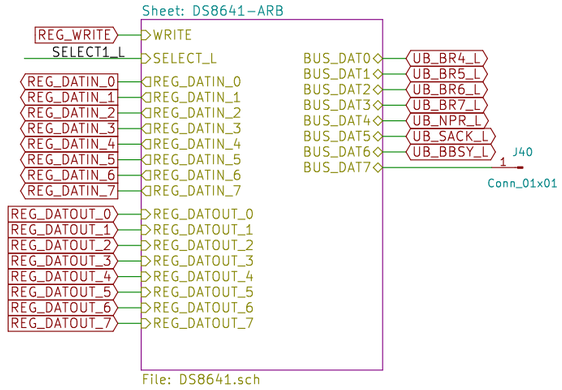
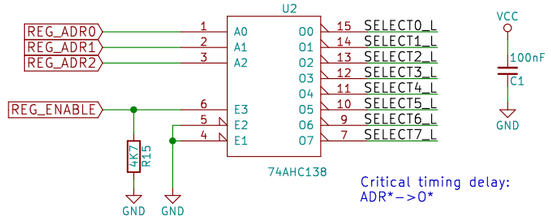




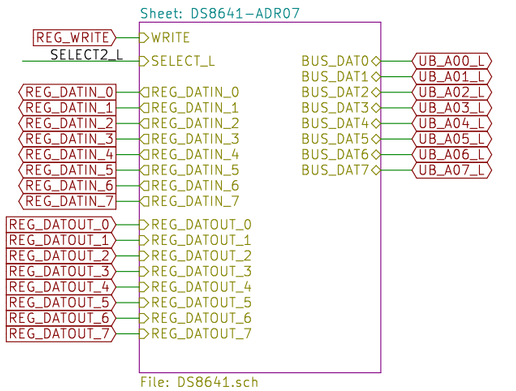


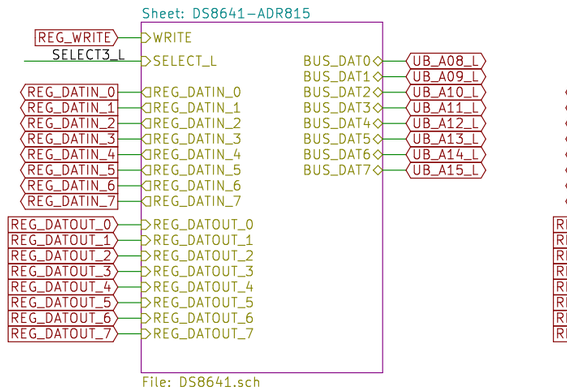
Unused driver pins on pin headers

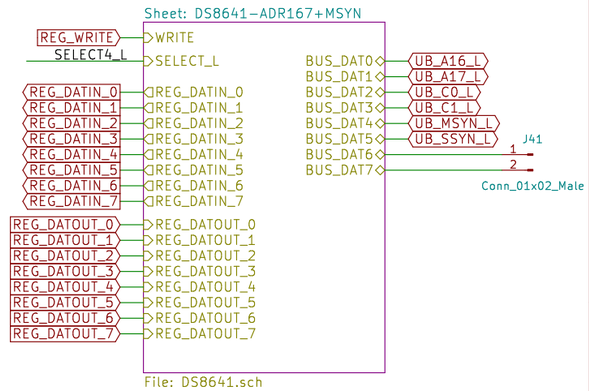


Critical timing delay:
ADR*->O*

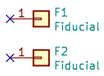
REG_ENABLE: The 74LVTH541 input latches must not drive the shared BBB SYSBOOT pins on power-up.







Optimization BBB: Dez 2019)
RN8,9 (DATIN) : 15 Ohm
RN10 <1:6>(REGADR): 0 Ohm
RN10 <7:8>(REGWRITE): 0 Ohm
R6,R7 (REGWRITE TERM): none
RN6,RN7 (DATOUT inline): 10
RN4,RN5 /DATOUT end) -> -/-



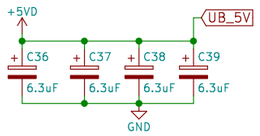
Sheet: /
File: unibone.sch

Title:

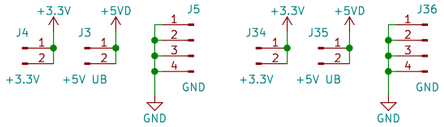
Size: A3	Date:	Rev:
KiCad E.D.A. kicad (5.1.4)-1		Id: 1/11

UNIBUS supply to BBB

UNIBUS supply to drivers

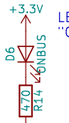


Supply bread board 1+2

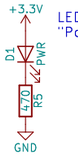


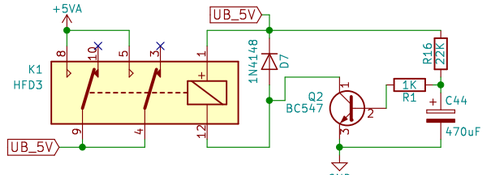
Implicite VCC is 3.3 V.
Generated on BBB.
+5V for drivers explicit

LED "On BUS"

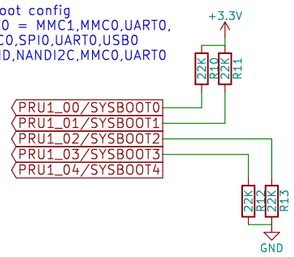


LED "Power"

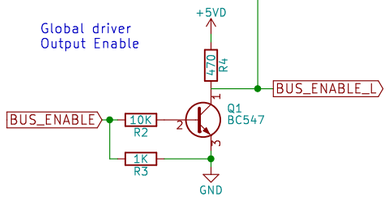




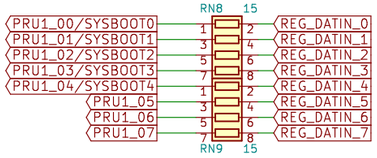
Override BBB boot config
Default: ...11100 = MMC1,MMC0,UART0,
...10111 = MMC0,SPI0,UART0,USB0
...10011 = NAND,NANDI2C,MMC0,UART0



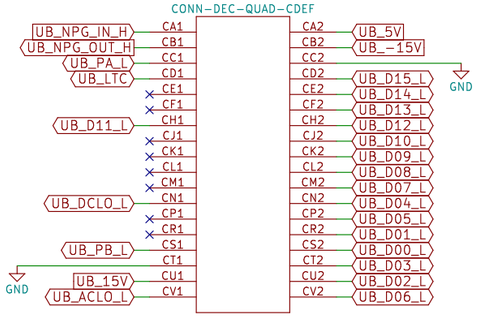
Global driver Output Enable



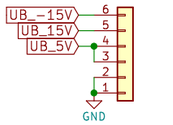
Use of PRU-EGPIOs:



J16
CONN-DEC-QUAD-CDEF

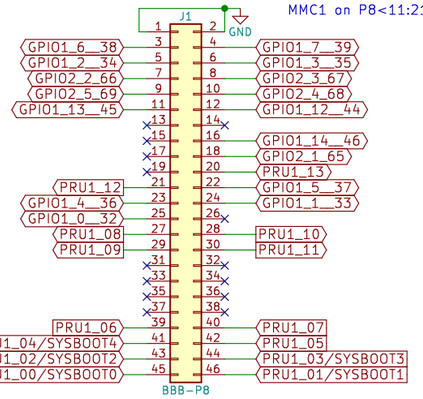


J60
Reichelt AKL 059-6

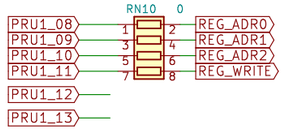


BBB Header:
use 2x25 pin footprint:
cabling 50 pins!

MMC1 on P8<11:21>

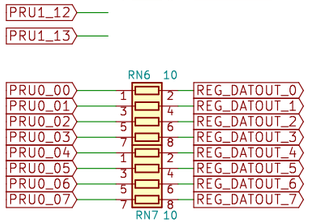


RN10 0

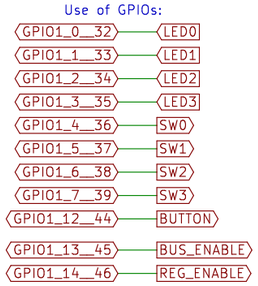


REGADR & WRITE both best at 0 Ohm

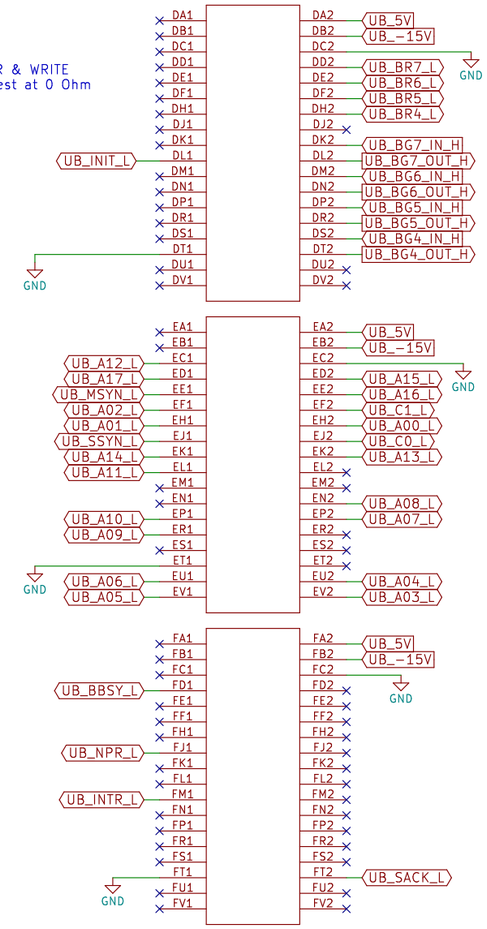
RN6 10



Use of GPIOs:

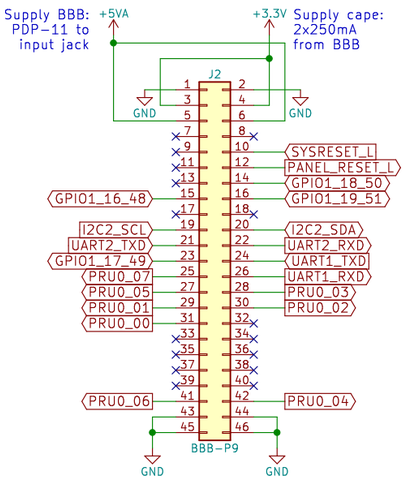


J16
CONN-DEC-QUAD-CDEF

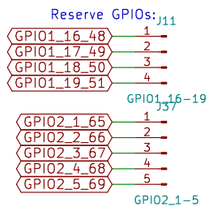


Supply BBB: PDP-11 to input jack

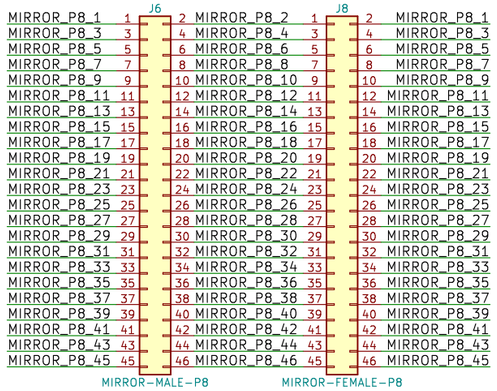
Supply cape: 2x250mA from BBB



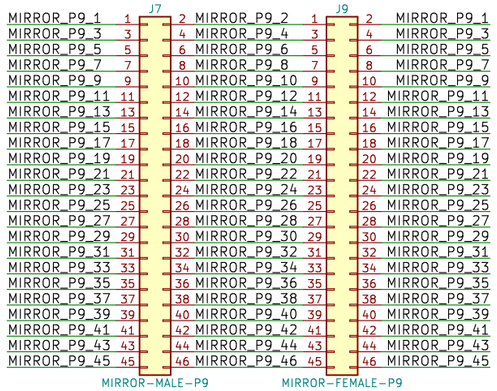
Reserve GPIOs:



J6 / J8



J7 / J9



Sheet: /pwr+interface/
File: pwr+interface.sch

Title:

Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.4)-1		Id: 2/11

Test–
LEDs

Test–
Switches

CAPE–EEPROM

TERM (opt)

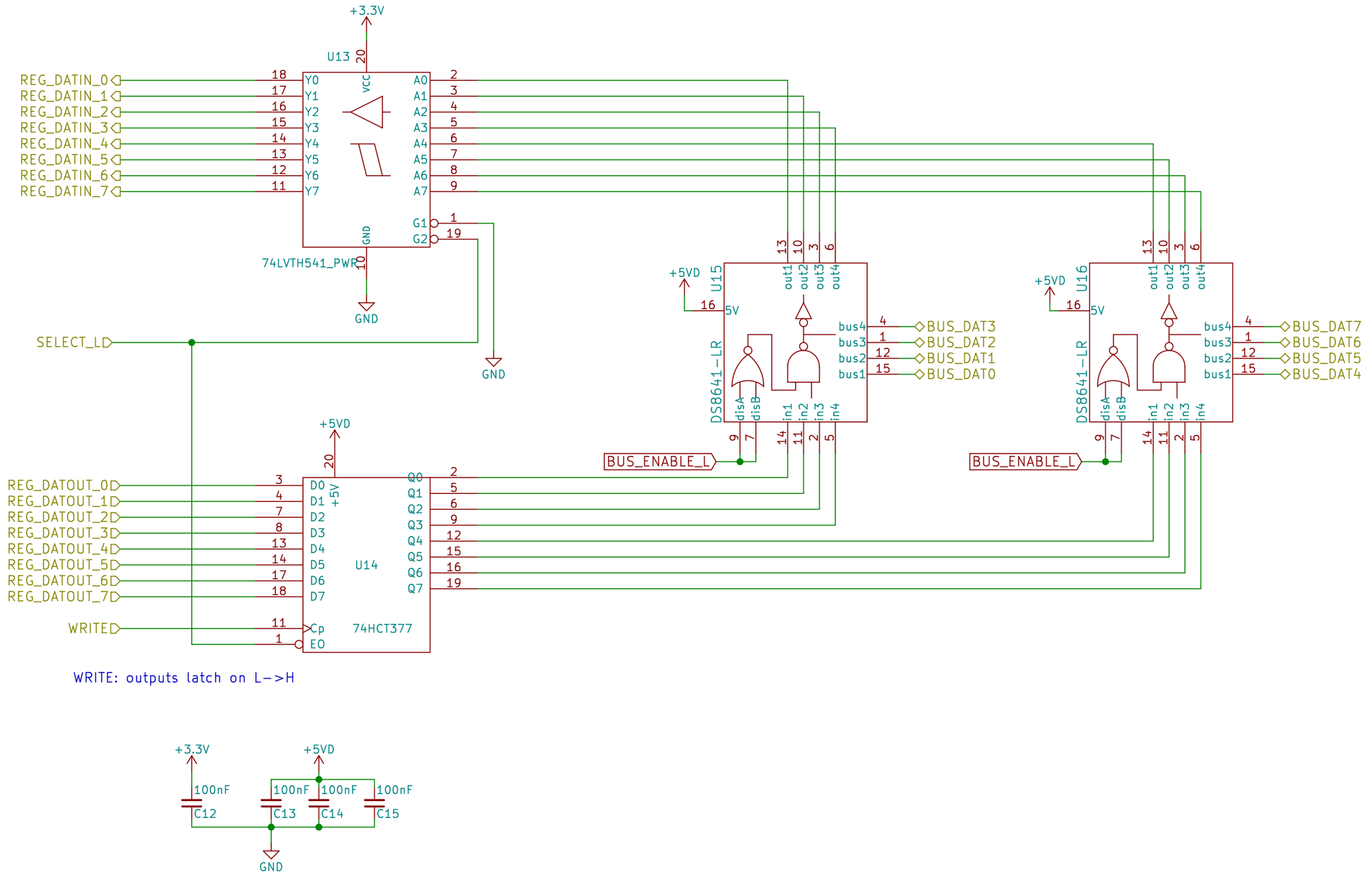
TERM (opt)

Panel over I2C2.
Unswitched 5V,
Pullups split,
2nd half on end of daisy chain.

BBB signal diagnostic

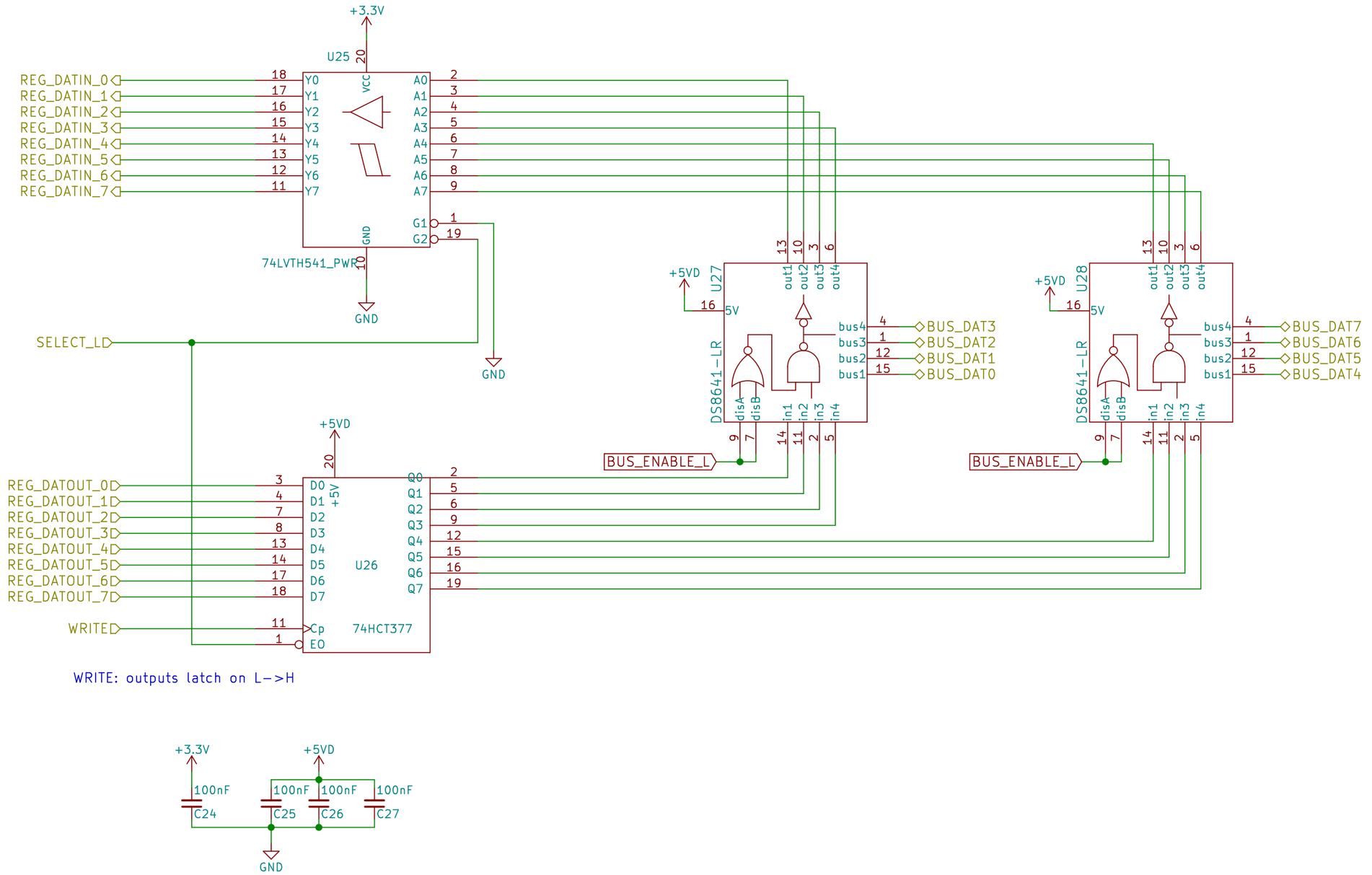
UNIBUS signal diagnostic

Sheet: /misc–io/	
File: misc–io.sch	
Title:	
Size: A4	Date:
KiCad E.D.A. kicad (5.1.4)–1	Id: 3/11



WRITE: outputs latch on L->H

Sheet: /DS8641-ADR815/		
File: DS8641.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.4)-1		Id: 4/11



WRITE: outputs latch on L->H

Sheet: /DS8641-ADR167+MSYN/		
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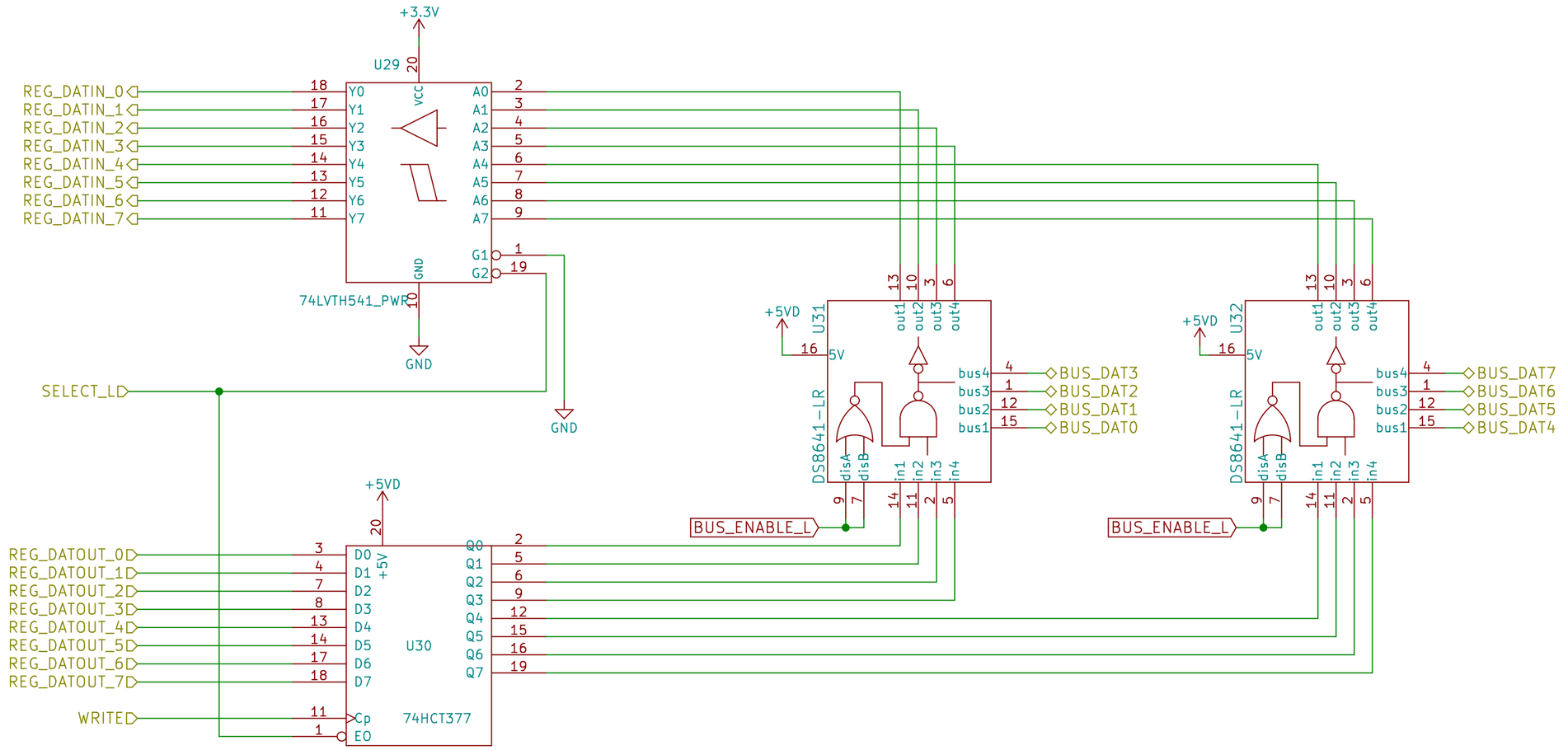
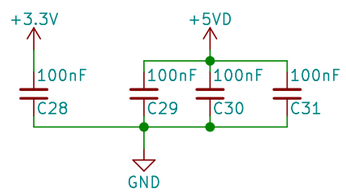
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.4)-1		Id: 5/11



WRITE: outputs latch on L->H



Sheet: /DS8641-ARB/		
File: DS8641.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.4)-1		Id: 6/11

SPC signals separated into IN and OUT wires.
TTL levels.

Extra 244 nicht nötig?
GRANT-IN-Signale nur 1 LOAD, std TTL?

U4 74LVTH541_PWR

REG_DATIN_0 REG_DATIN_1 REG_DATIN_2 REG_DATIN_3 REG_DATIN_4 REG_DATIN_5 REG_DATIN_6 REG_DATIN_7

U6 74LS244_5V

BUS_IN_DAT0 BUS_IN_DAT1 BUS_IN_DAT2 BUS_IN_DAT3 BUS_IN_DAT4 BUS_IN_DAT5 BUS_IN_DAT6 BUS_IN_DAT7

SELECT_LD

U8 DS8641-LR

BUS_OUT_DAT3 BUS_OUT_DAT2 BUS_OUT_DAT1 BUS_OUT_DAT0

BUS_ENABLE_L

U5 74HCT377

REG_DATOUT_0 REG_DATOUT_1 REG_DATOUT_2 REG_DATOUT_3 REG_DATOUT_4 REG_DATOUT_5 REG_DATOUT_6 REG_DATOUT_7

WRITE

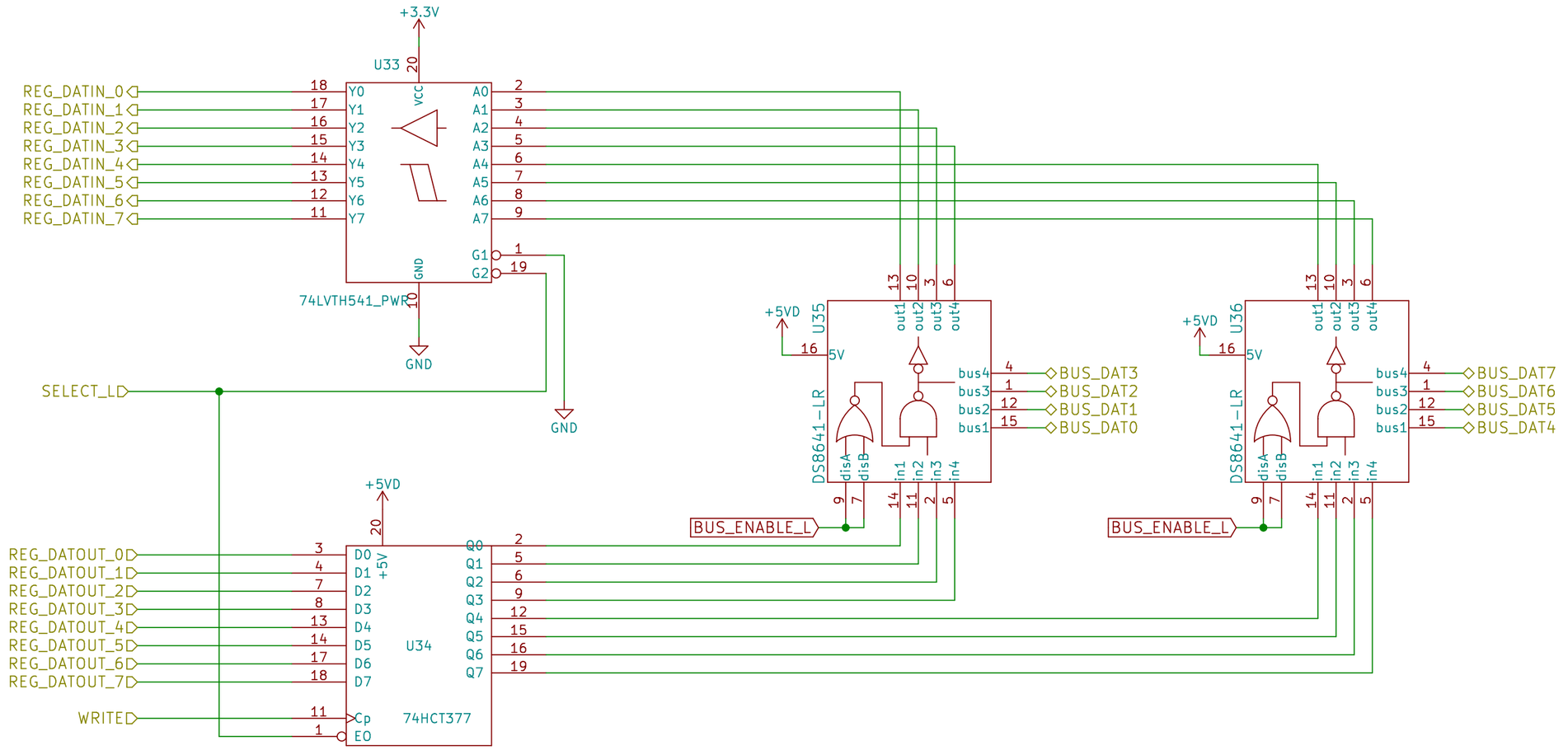
WRITE: outputs latch on L->H

U7 DS8641-LR

BUS_OUT_DAT7 BUS_OUT_DAT6 BUS_OUT_DAT5 BUS_OUT_DAT4

C3 C4 C5 C6 C7 100nF

Sheet: /TTL_IN_OUT/		
File: TTL_IN_OUT.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.4)-1		Id: 7/11



Sheet: /DS8641-SSYN+MISC/		
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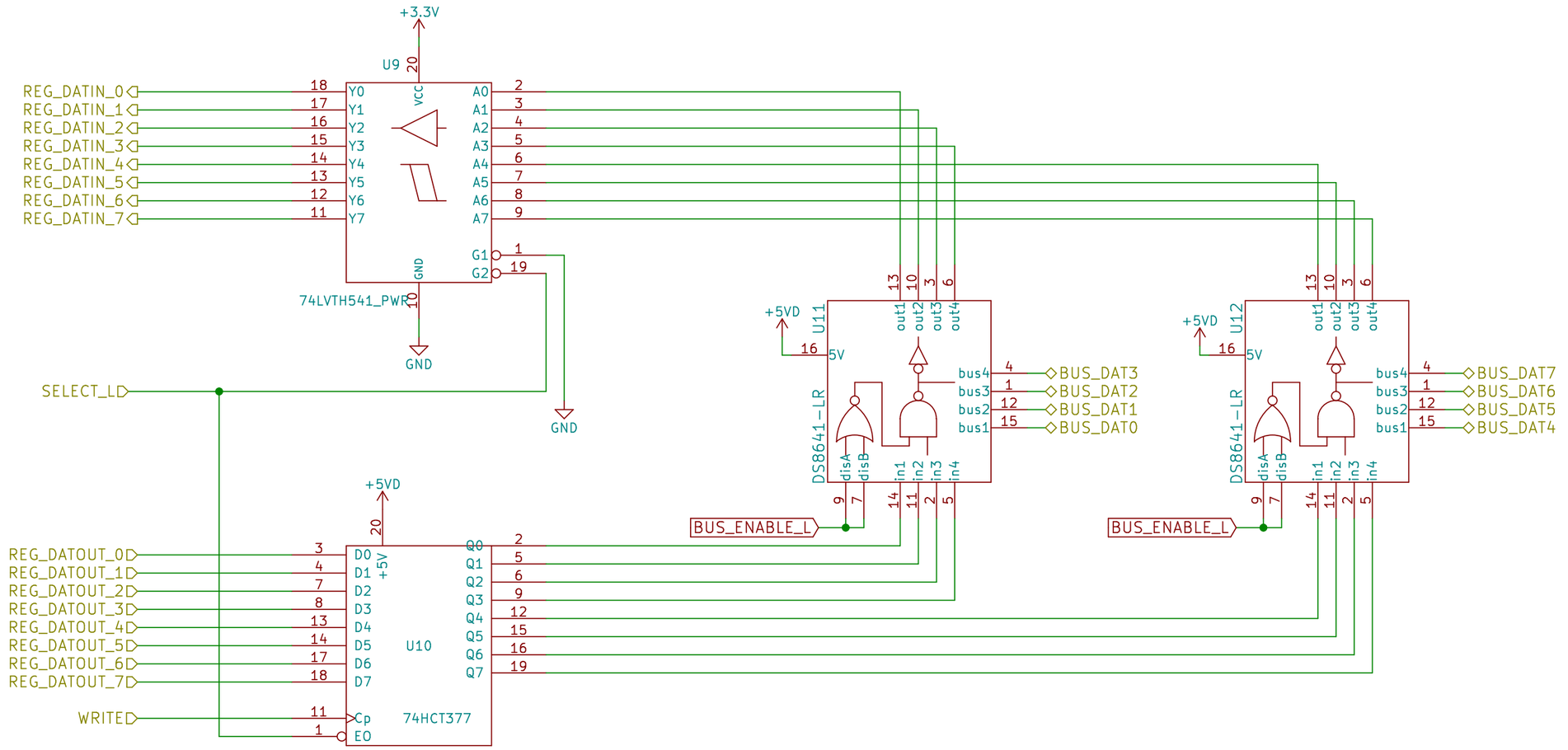
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.4)-1		Id: 8/11



Sheet: /DS8641-ADR07/		
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Title:		
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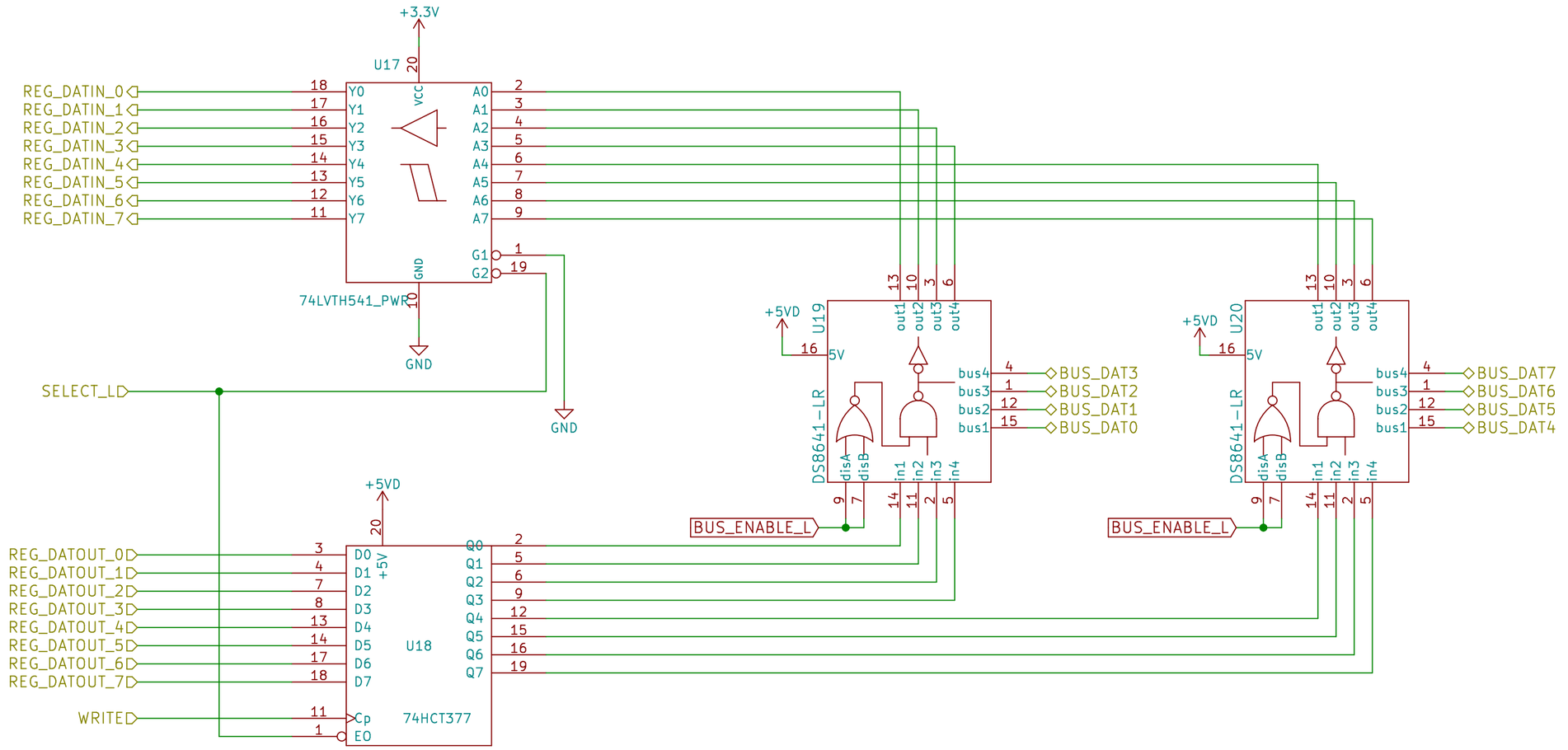
KiCad E.D.A. kicad (5.1.4)-1		Id: 9/11



Sheet: /DS8641-DAT07/		
File: DS8641.sch		
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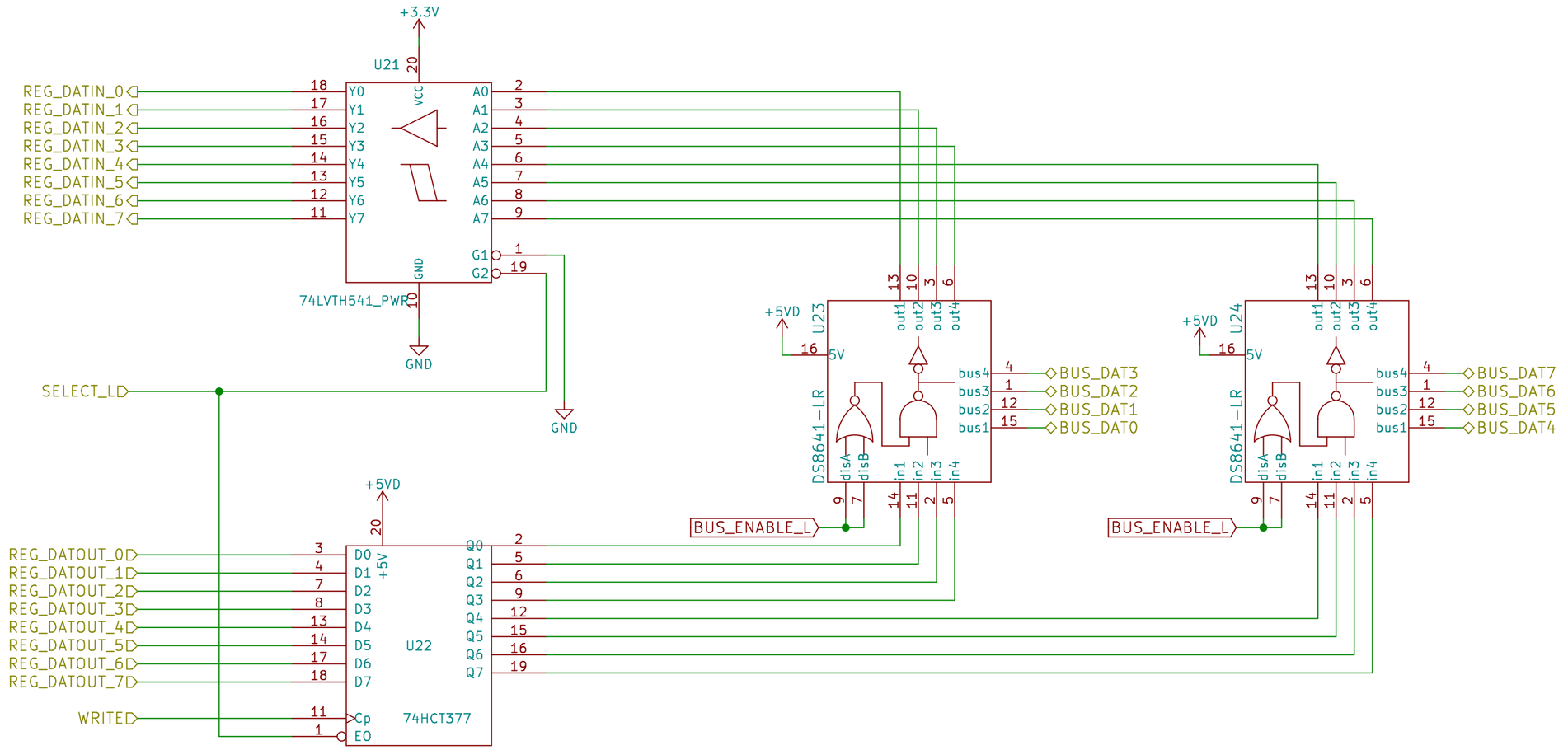
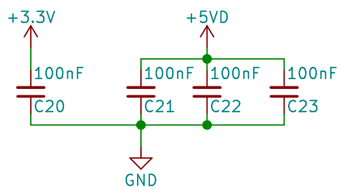
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.4)-1		Id: 10/11



WRITE: outputs latch on L->H



Sheet: /DS8641-DAT815/		
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KiCad E.D.A. kicad (5.1.4)-1		Id: 11/11