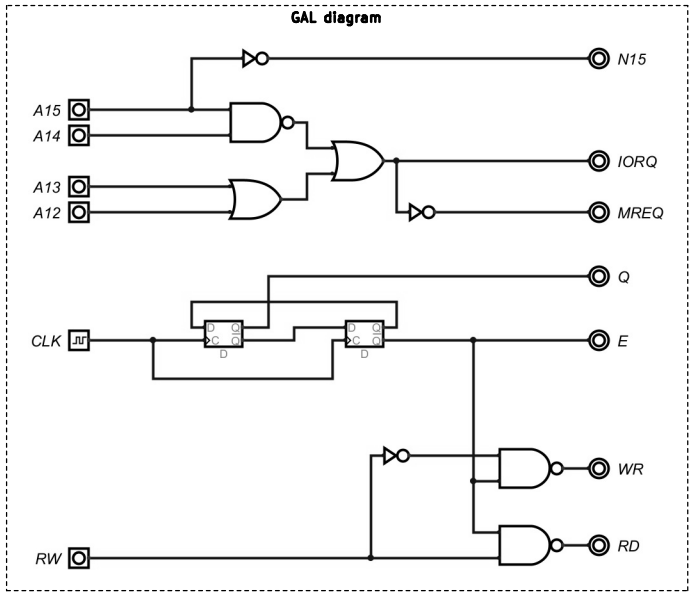

Tadeusz Pycio

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Title: HD63C09E/MC6809E

Size: A4	Date:	Rev: 1.0
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- **NOTE FOR USE**
- **Execution Sequence of CLR Instruction**

Example: CLR (Extended)

$8000	CLR	$A000
$A000	FCB	$80

Cycle #	Address	Data	R/$\overline{W}$	Description
1	8000	7F	1	Opcode Fetch
2	8001	A0	1	Operand Address, High Byte
3	8002	00	1	Operand Address, Low Byte
4	FFFF	*	1	$\overline{VMA}$ Cycle
5	A000	80	1	Read the Data
6	FFFF	*	1	$\overline{VMA}$ Cycle
7	A000	00	0	Store Fixed "00" into Specified Location

* The data bus has the data at that particular address.

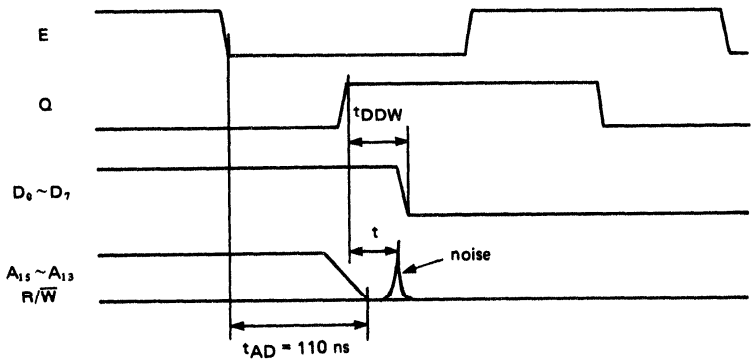
Cycle-by-cycle flow of CLR instruction (Direct, Extended, Indexed Addressing Mode) is shown below. In this sequence the content of the memory location specified by the operand is read before writing "00" into it. Note that status Flags, such as IRQ Flag, will be cleared by this extra data read operation when accessing the control/status register (sharing the same address between read and write) of peripheral devices.

- **The Noise of HD6309E at Bus Outputs Changing**

We shall notify you of the noise of the HD6309E.

The noise over 0.8V may appear on the output signals when data bus or address bus outputs change from "High" to "Low". Problems and countermeasure are shown as follows.

(1) The Noise at Data Bus Outputs Changing ("High→"Low")
Problem: The noise over 0.8V may appear on A_{15}~A_{13}, R/W outputs change (worst case; $FF→$00) as shown in Figure 19.



Noise peak (worst case); about 1.5V
Test condition
Ta = −20°C
V_{CC} = 5.5V
Number of data bus lines switching from "High" to "Low" = 8
($FF→$00) data bus load capacitance = 130pF

Period of the noise occurrence (reference data)

t = 6~34ns (Ta = −20°C)
t = 8~43ns (Ta = 25°C)
t = 12~54ns (Ta = 75°C)

Figure 19 Noise at data bus output changing

Countermeasure: If the noise level can not be reduced by controlling data bus load capacitance or reducing V_{CC} in your application system, connect damping resistors (about 100~150Ω) to data bus to reduce the noise level as shown in Figure 20. Table 11 shows the relationship between damping resistors and electrical characteristics. Connecting damping resistors to data bus is effective to reduce the noise level as shown in Figure 21.

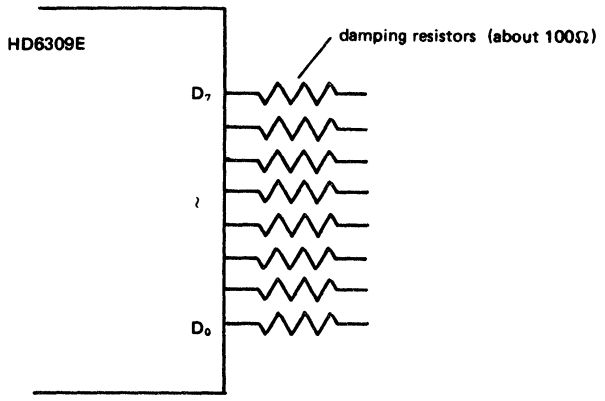


Figure 20 Connecting damping resistors to data bus

Table 11 The relationship between damping resistors and electrical characteristics

			R = 0Ω	R = 100 ~ 150Ω
HD63B09E (2MHz)	t_{DHW}	Ta = −20~0°C	20 ns	10 ns
		Ta = 0~75°C	30 ns	15 ns
HD63C09E (3MHz)	t_{DDW}		70 ns	80 ns
	t_{DHW}	Ta = −20~0°C	20 ns	10 ns
		Ta = 0~75°C	30 ns	15 ns