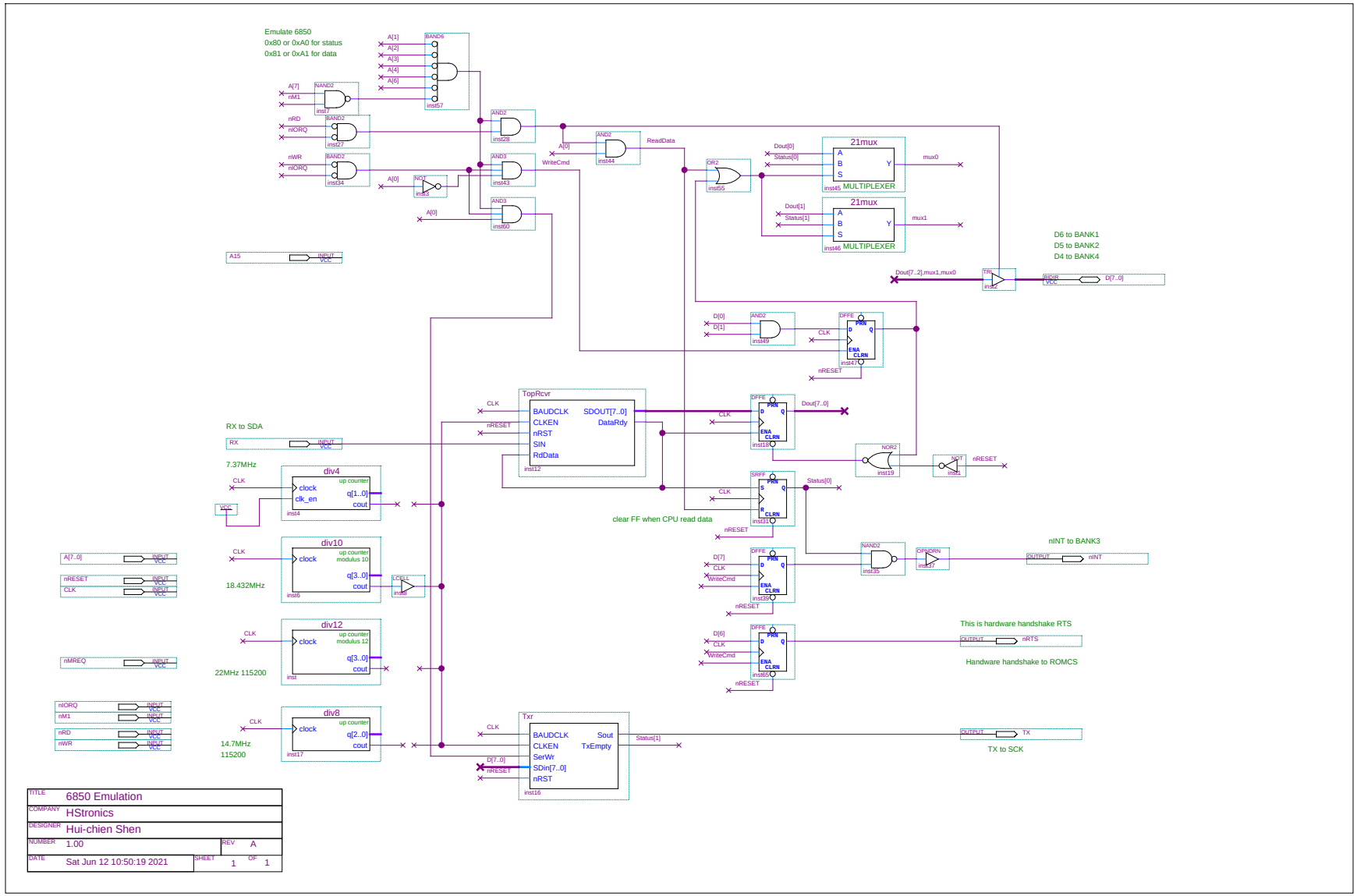
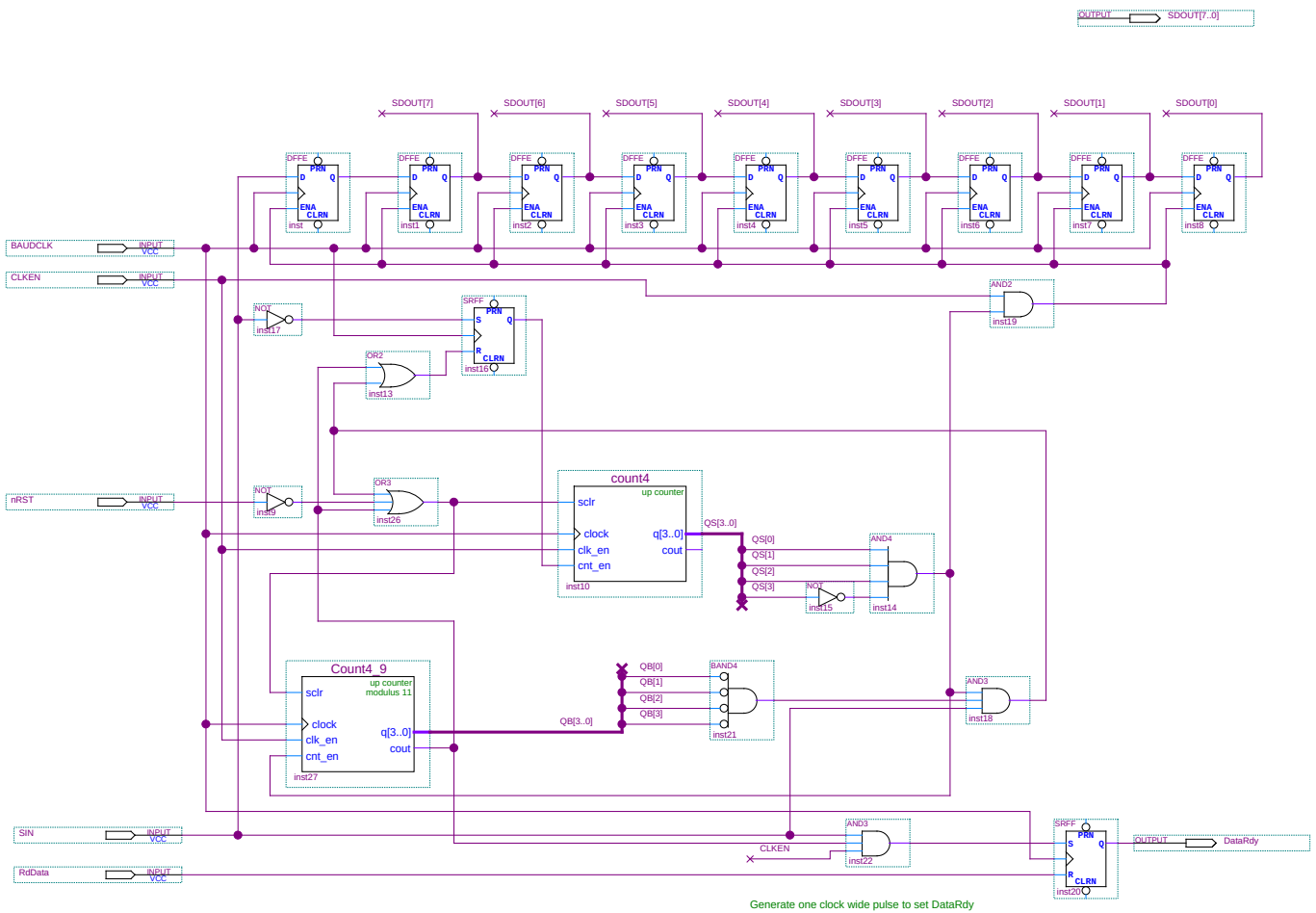
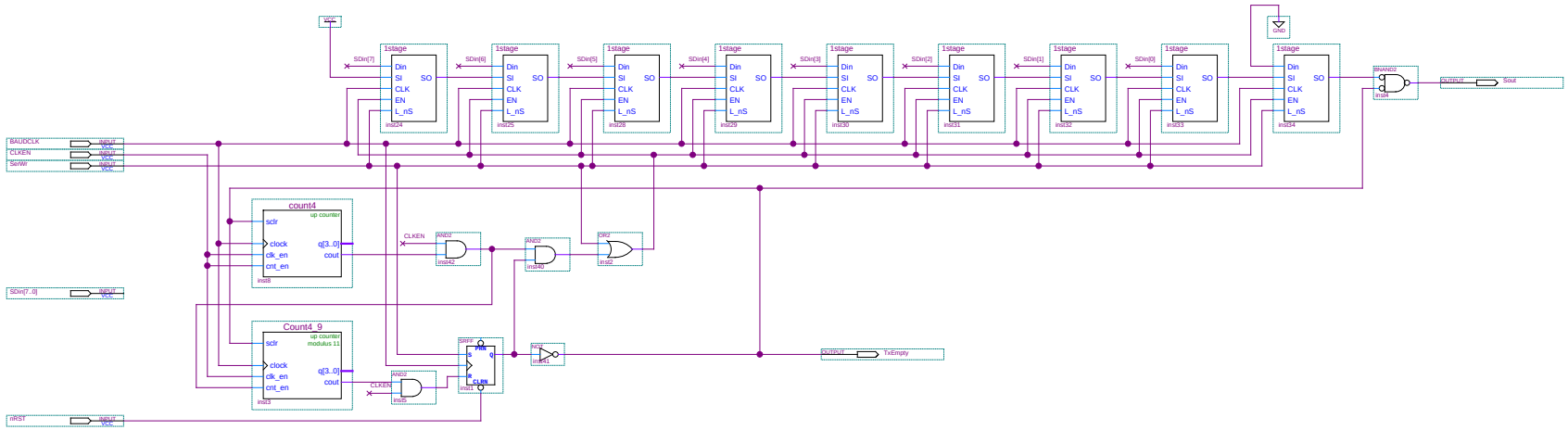

Emulate 6850
0x80 or 0xA0 for status
0x81 or 0xA1 for data
21mux
MULTIPLEXER
D6 to BANK1
D5 to BANK2
D4 to BANK4
TopRcvr
BAUDCLK
CLKEN
nRST
SIN
RdData
SDOUT[7..0]
DataRdy
RX to SDA
7.37MHz
div4
div10
div12
div8
18.432MHz
22MHz 115200
14.7MHz
115200
clear FF when CPU read data
nINT to BANK3
This is hardware handshake RTS
Handware handshake to ROMCS
Txr
Sout
TxEmpty
TX to SCK
TITLE 6850 Emulation
COMPANY HStronics
DESIGNER Hui-chien Shen
NUMBER 1.00
REV A
DATE Sat Jun 12 10:50:19 2021
SHEET 1 OF 1



Generate one clock wide pulse to set DataRdy
Because DataRdy may generate an interrupt. If interrupt service occurred too quickly, the flipflop may still be setting while RdData is resetting it.

TITLE	Serial Receiver, 8N1		
COMPANY	HCStronics		
DESIGNER	Bill Shen		
NUMBER	1.00	REV	A
DATE	Sun Jun 24 15:49:51 2018	SHEET 1	OF 1



Generate only one clock wide pulse to assert TxEmpty flag
Because TxEmpty may generate an interrupt. If interrupt service occurred too quickly,
the flipflop may still be resetting while SerWr is setting it.

TITLE	Serial Transmitter, 8N1		
COMPANY	HCStronics		
DESIGNER	Bill Shen		
NUMBER	1.00	REV	A
DATE	Sun Jun 24 15:49:36 2018	SHEET	1 OF 1