P1
RCBUS-80 MALE

U1
Flash 512k
SST39SF040

U2
Flash 512k
SST39SF040

U3
RAM 512k
AS6C4008

JP1
Flash Write Enable

U4.1
74AHCT139

U4.2
74AHCT139

JP2, JP3 amd JP4 enable memory to be mapped with either ROM at the bottom of memory (Low memory) and RAM at the top of memory (High memory) as required by Z80 CPU, or RAM at the bottom of memory and ROM at the top

RN1
8x100k
(optional)

R1
10k

SW1
Flash select
Flash #2
Flash #1

SW1
switch
casing

JP5
Flash 1

Fit either JP5 or SW1

Jumper JP2:2-3 (RAM Hi)
Jumper JP3:1-2 (ROM 1 Lo)
Jumper JP4:1-2 (ROM 2 Lo)
ROM 0x00000 to 0x7FFFF
RAM 0x80000 to 0xFFFFF

Jumper JP2:1-2 (RAM Lo)
Jumper JP3:2-3 (ROM 1 Hi)
Jumper JP4:2-3 (ROM 2 Hi)
RAM 0x00000 to 0x7FFFF
ROM 0x80000 to 0xFFFFF

Resistor RN1 is optional and provides either pull-up or pull-down of A16 to A23.
In the position indicated it provides pull-up.
In the reverse position it provides pull-down.

U4
74AHCT139

C1 100nF
C2 100nF
C3 100nF
C4 100nF
C5 100uF

Memory module with 512kB RAM and two 512kB Flash ROM arranged as a single flat 1MB bank
An 8-bit processor with a 16-bit address bus will require a memory management to generate the required 20-bit address bus

Title:	SC721: Memory 512k RAM + 512k ROM	Schematic: v1.0.0
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