

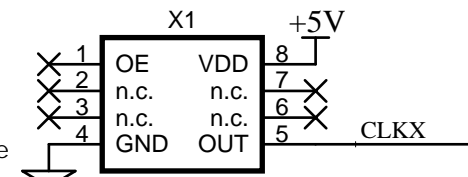
U2.1 is required to maintain software compatibility with RC2014 systems

JP5 selects the baud rate clock for port A
 JP5.1 = Bus clock 2 (CLK2)
 JP5.2 = CTC input clock (CLKC)
 JP5.3 = CTC channel 0 output

JP6 selects the baud rate clock for port B
 JP6.1 = Bus clock 2 (CLK2)
 JP6.2 = CTC input clock (CLKC)
 JP6.3 = CTC channel 1 output

JP4 selects the clock source for the CTC channels (CLKC)
 JP4.1 = Bus clock (CLK)
 JP4.2 = Bus clock 2 (CLK2)
 JP4.3 = Oscillator X1 (CLKX)

WARNING
 CLKX must be less than half the frequency of the CPU clock CLK due to internal synchronisation of the CTC. See CTC datasheet.



Optional clock source typically 7.3728 MHz

CTC functions
 Channel 0: baud rate generator for SIO port A (optional with JP5)
 Channel 1: baud rate generator for SIO port B (optional with JP6)
 Channel 2: timer low byte
 Channel 3: timer high byte

Title:	SC725 SIO and CTC for RCBus	Schematic:	v1.0.0	
Date:	2023-08-08	Created:	2023-08-05	
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