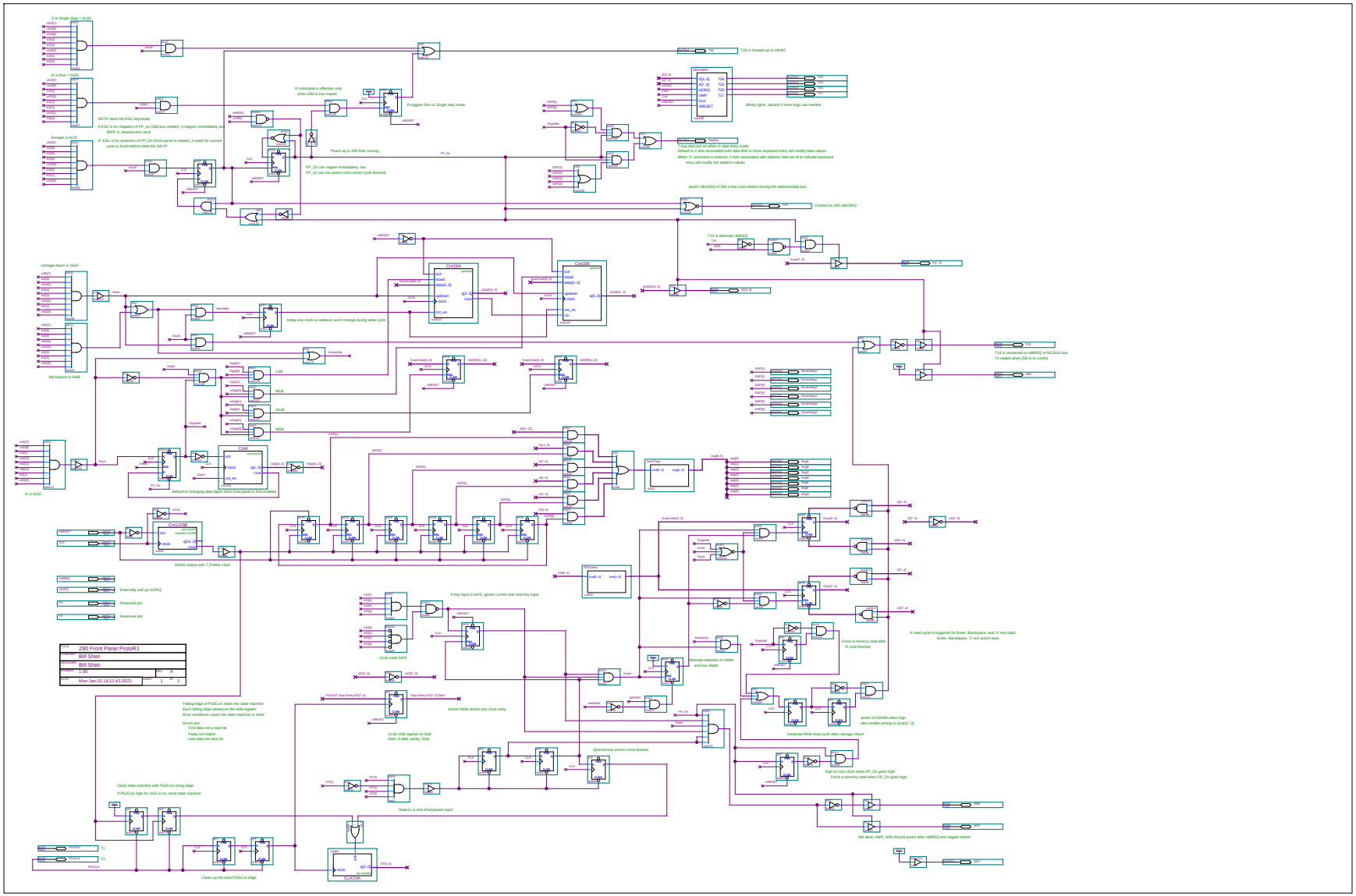
S is Single Step = 0x1B
R is Run = 0x2D
Escape is 0x76
SR-FF latch the ESC keystroke
If ESC is for negation of FP_on (Z80 bus master), it happen immediately and SRFF is cleared next clock
IF ESC is for assertion of FP_On (front panel is master), it waits for current cycle to finish before clear the SR-FF
R command is effective only when Z80 is bus master
R toggles Run or Single step mode
Power up to Z80 free running
FP_On can negate immediately, but FP_on can not assert until current cycle finished
T28 is hooked up to nWAIT
Blinky lights, discard if more logic are needed
T-reg data are on when in data entry mode
Default to 2 dots associated with data field to show keyboard entry will modify data values
when 'X' command is entered, 4 dots associated with address field are lit to indicate keyboard entry will modify the address values
assert nIUSRQ of Z80 a few clock before driving the address/data bus
Connect to Z80 nIUSRQ
T19 is alternate nMREQ
carriage return is 0x5A
Delay one clock so address won't change during write cycle
Backspace is 0x66
T19 is connected to nMREQ of RC2014 bus
Tri-stated when Z80 is in control
'X' is 0x22
Default to changing data digits when front panel is first enabled
600Hz output with 7.37MHz clock
Externally pull up nIORQ
Reserved pin
Reserved pin
Z80 Front Panel ProtoR1
Bill Shen
Bill Shen
1.00
Mon Jan 02 16:12:43 2023
If key input is 0xFD, ignore current and next key input
Scan code 0xF0
Alternate between hi nibble and low nibble
A read cycle is triggered for Enter, Backspace, and 'X' key input
Enter, Backspace, 'X' are action keys
Force a memory read after 'X' cmd finished
Falling edge of PS2CLK starts the state machine
Each falling edge advances the shift register
Error conditions cause the state machine to reset
Errors are:
Find data not a start bit
Parity not match
Last data not stop bit
Assert Write strobe one clock early
11-bit shift register to hold Start, 8 data, parity, Stop
Synchronize across clock domain
Generate RAM read cycle after carriage return
assert nCSRAM when high also enable writing to Scan[7..0]
Clock state machine with PS2CLK rising edge
If PS2CLK high for 1mS or so, reset state machine
State11 is end of keyboard input
Clean up the slow PS2CLK edge
high for one clock when FP_On goes high
Force a memory read when FP_On goes high
Not ideal, nMR, nRD should assert after nMREQ and negate before