SCK shifts SER into shift register on rising edge.
RCK registers data to output on rising edge.

Count/Load on rising edge of CLK

CLK shifts data on rising edge
SH/LD is transparent load

State	Next
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	12 (15 If /SER_WR = 0)
*9	12 (15 If /SER_WR = 0)
*10	12 (15 If /SER_WR = 0)
*11	12 (15 If /SER_WR = 0)
12	12 (15 If /SER_WR = 0)
*13	12 (15 If /SER_WR = 0)
*14	12 (15 If /SER_WR = 0)
15	15 (0 If /SER_WR = 1)

*not reached

Max CLK frequency with 74LS163 is 12MHz.
For 20MHz, 74ALS163 may be used.

Use;-
IN A,(C) (12 clock cycles)
INI (12 + 4 clock cycles)
INIR (12 + 4 + (5) clock cycles)

Note.
IN A,(nn) (11 clock cycles)
May not be reliable above 12MHz.

WR-ADR Output data and transfer (Y0)
RD-ADR Read data without transfer (Y2)
RD-ADR+1 Read data with transfer (Y3)

WR-ADR+2 Output control (Y4)
RD-ADR+2 Read status (Y6)

Typically U1A to U4A will be inputs from previous card and U1B to U4B will be outputs to the next card.

If not used they may be linked.

Fit resistor if 683/689

Fit link for 688/689

Default base address 0x1C

Fit _RN1 unless 682 is used

LED1 and LED2 low current type, select R1 and R3 to suit.

U1 SOT 223, 3.3v Low drop out regulator

C1 and C3 = 10uF LCSC.COM C9807 CL31A106KAHNNNE
Multilayer Ceramic Capacitors MLCC - SMD/SMT 10uF 25V 1206 RoHS
Check datasheet for U1 decoupling requirement

TITLE:	RC2014_SPI_WIZNET
Document Number:	REV:
Date: 11/05/2019 18:03	Sheet: 1/1