

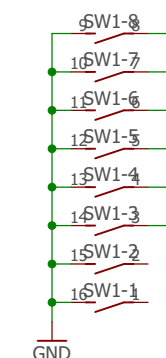
State	Next
0	1
1	2
2	3
3	4
4	5
5	6
6	7
7	8
8	12 (15 If /SER_WR = 0)
*9	12 (15 If /SER_WR = 0)
*10	12 (15 If /SER_WR = 0)
*11	12 (15 If /SER_WR = 0)
12	12 (15 If /SER_WR = 0)
*13	12 (15 If /SER_WR = 0)
*14	12 (15 If /SER_WR = 0)
15	15 (0 If /SER_WR = 1)

\*not reached

P1-1	A15
P1-2	A14
P1-3	A13
P1-4	A12
P1-5	A11
P1-6	A10
P1-7	A9
P1-8	A8
P1-9	A7
P1-10	A6
P1-11	A5
P1-12	A4
P1-13	A3
P1-14	A2
P1-15	A1
P1-16	A0
P1-17	GND
P1-18	VCC
P1-19	/RFSH
P1-20	PAGE
P1-21	CK2
P1-22	/BUSAK
P1-23	/HALT
P1-24	/BUSRQ
P1-25	/WAIT
P1-26	/IORQ
P1-27	D0
P1-28	D1
P1-29	D2
P1-30	D3
P1-31	D4
P1-32	D5
P1-33	D6
P1-34	D7
P1-35	U1B
P1-36	U2B
P1-37	U3B
P1-38	U4B
P1-39	IF
P2-1	GND
P2-2	VCC
P2-3	/RFSH
P2-4	PAGE
P2-5	CK2
P2-6	/BUSAK
P2-7	/HALT
P2-8	/BUSRQ
P2-9	/WAIT
P2-10	/NMI

Typically U1A to U4A will be inputs from previous card and U1B to U4B will be outputs to the next card.

If not used they may be linked.

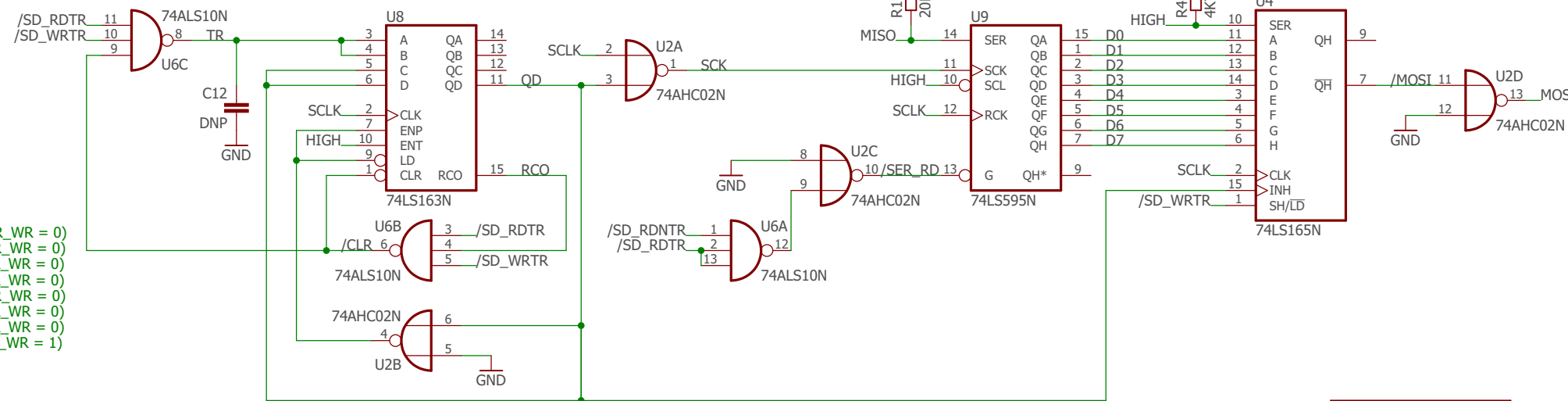


Fit\_RN1 unless 682 is used

SCK shifts SER into shift register on rising edge.  
RCK registers data to output on rising edge.

CLK shifts data on rising edge  
SH/LD is transparent load

Count/Load on rising edge of CLK



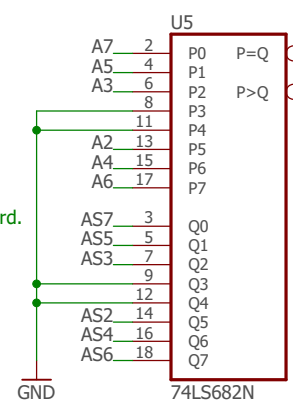
Max CLK frequency with 74LS163 is 12MHz.  
For 20MHz, 74ALS163 may be used.

Use:-  
IN A,(C) (12 clock cycles)  
INI (12 + 4 clock cycles)  
INIR (12 + 4 + (5) clock cycles)

Note.  
IN A,(nn) (11 clock cycles)  
May not be reliable above 12MHz.

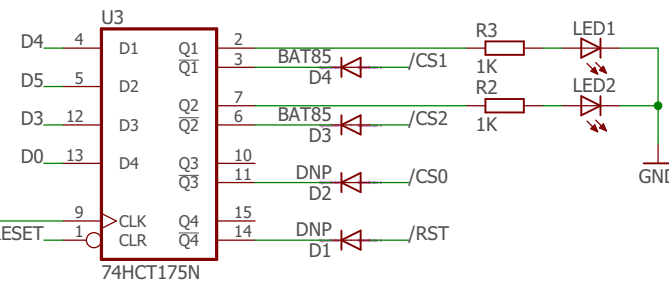
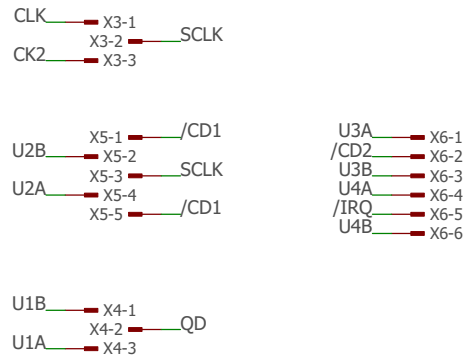
WR-ADR Output data and transfer (Y0)  
RD-ADR Read data without transfer (Y2)  
RD-ADR+1 Read data with transfer (Y3)  
WR-ADR+2 Output control (Y4)  
RD-ADR+2 Read status (Y6)

Fit resistor if 683/689

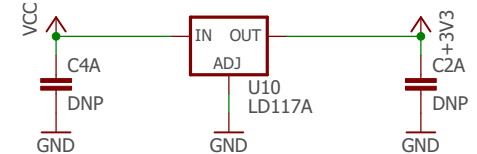


Fit link for 688/689

Default base address 0x1C

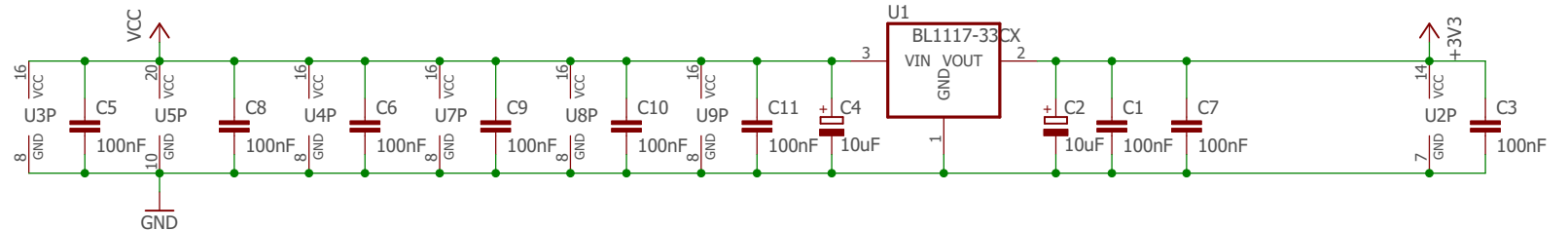


LED1 and LED2 low current type,  
select R1 and R3 to suit.



U1 SOT 223, 3.3v Low drop out regulator

C1 and C3 = 10uF LCSC.COM C9807 CL31A106KAHNNNE  
Multilayer Ceramic Capacitors MLCC - SMD/SMT 10uF 25V 1206 RoHS  
Check datasheet for U1 decoupling requirement



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