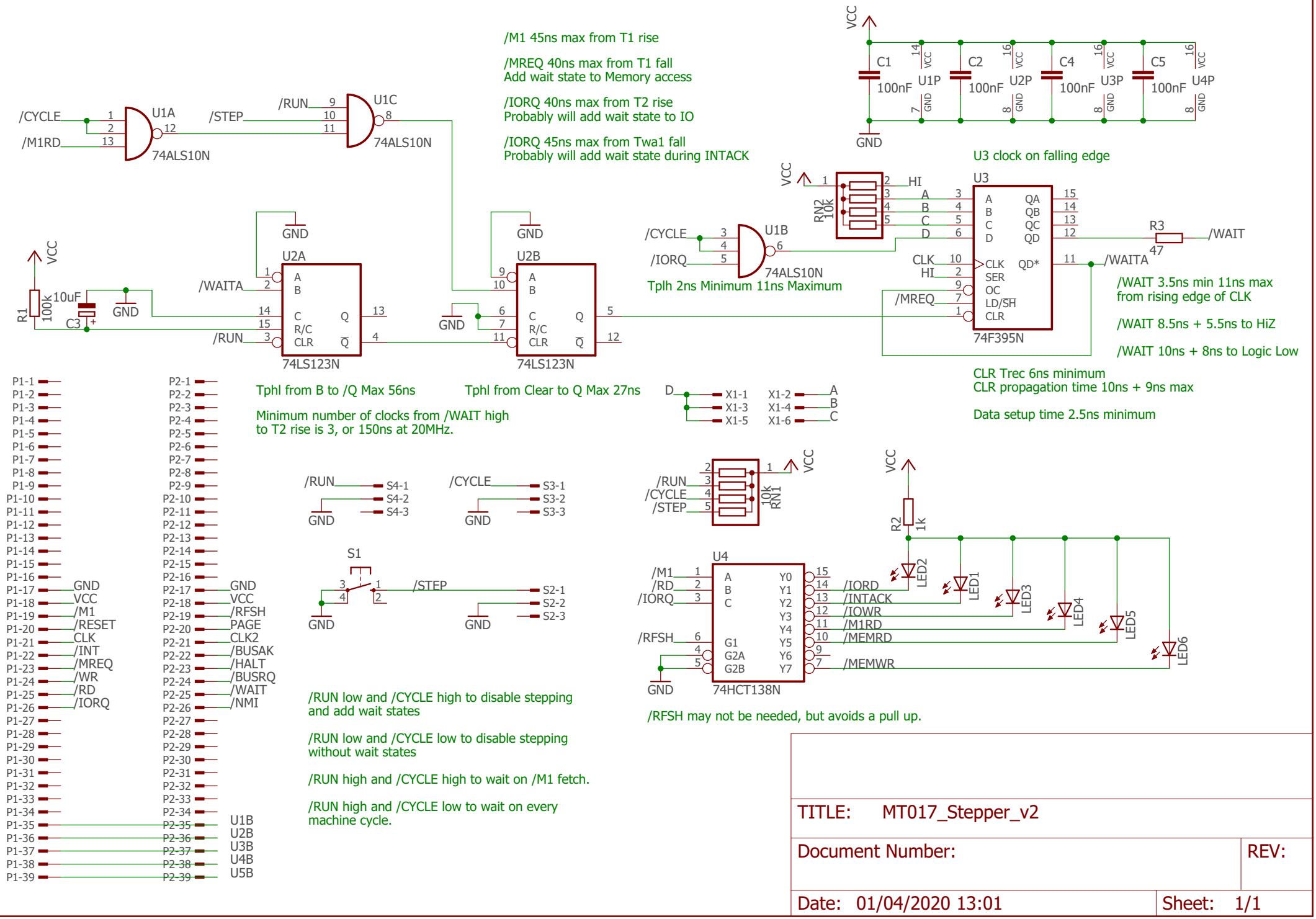
/M1 45ns max from T1 rise
/MREQ 40ns max from T1 fall
Add wait state to Memory access
/IORQ 40ns max from T2 rise
Probably will add wait state to IO
/IORQ 45ns max from Twa1 fall
Probably will add wait state during INTACK
U3 clock on falling edge
/CYCLE
/M1RD
/STEP
/RUN
U1A
U1B
U1C
74ALS10N
VCC
GND
C1
C2
C4
C5
100nF
U1P
U2P
U3P
U4P
R1
100k
10uF
C3
U2A
U2B
/WAITA
74LS123N
Tplh 2ns Minimum 11ns Maximum
RN2
10k
HI
U3
74F395N
R3
47
/WAIT
/MREQ
CLK
Tphl from B to /Q Max 56ns
Tphl from Clear to Q Max 27ns
/WAIT 3.5ns min 11ns max
from rising edge of CLK
/WAIT 8.5ns + 5.5ns to HiZ
/WAIT 10ns + 8ns to Logic Low
CLR Trec 6ns minimum
CLR propagation time 10ns + 9ns max
Data setup time 2.5ns minimum
Minimum number of clocks from /WAIT high
to T2 rise is 3, or 150ns at 20MHz.
P1-1
P1-2
P1-3
P1-4
P1-5
P1-6
P1-7
P1-8
P1-9
P1-10
P1-11
P1-12
P1-13
P1-14
P1-15
P1-16
P1-17 GND
P1-18 VCC
P1-19 /M1
P1-20 /RESET
P1-21 CLK
P1-22 /INT
P1-23 /MREQ
P1-24 /WR
P1-25 /RD
P1-26 /IORQ
P1-27
P1-28
P1-29
P1-30
P1-31
P1-32
P1-33
P1-34
P1-35 U1B
P1-36 U2B
P1-37 U3B
P1-38 U4B
P1-39 U5B
P2-1
P2-2
P2-3
P2-4
P2-5
P2-6
P2-7
P2-8
P2-9
P2-10
P2-11
P2-12
P2-13
P2-14
P2-15
P2-16
P2-17 GND
P2-18 VCC
P2-19 /RFSH
P2-20 PAGE
P2-21 CLK2
P2-22 /BUSAK
P2-23 /HALT
P2-24 /BUSRQ
P2-25 /WAIT
P2-26 /NMI
P2-27
P2-28
P2-29
P2-30
P2-31
P2-32
P2-33
P2-34
P2-35
P2-36
P2-37
P2-38
P2-39
D
X1-1
X1-2
X1-3
X1-4
X1-5
X1-6
A
B
C
/RUN
/CYCLE
/STEP
S4-1
S4-2
S4-3
S3-1
S3-2
S3-3
S1
S2-1
S2-2
S2-3
RN1
10k
R2
1k
U4
74HCT138N
/M1
/RD
/IORQ
/RFSH
/IORD
/INTACK
/IOWR
/M1RD
/MEMRD
/MEMWR
LED1
LED2
LED3
LED4
LED5
LED6
/RUN low and /CYCLE high to disable stepping
and add wait states
/RUN low and /CYCLE low to disable stepping
without wait states
/RUN high and /CYCLE high to wait on /M1 fetch.
/RUN high and /CYCLE low to wait on every
machine cycle.
/RFSH may not be needed, but avoids a pull up.
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