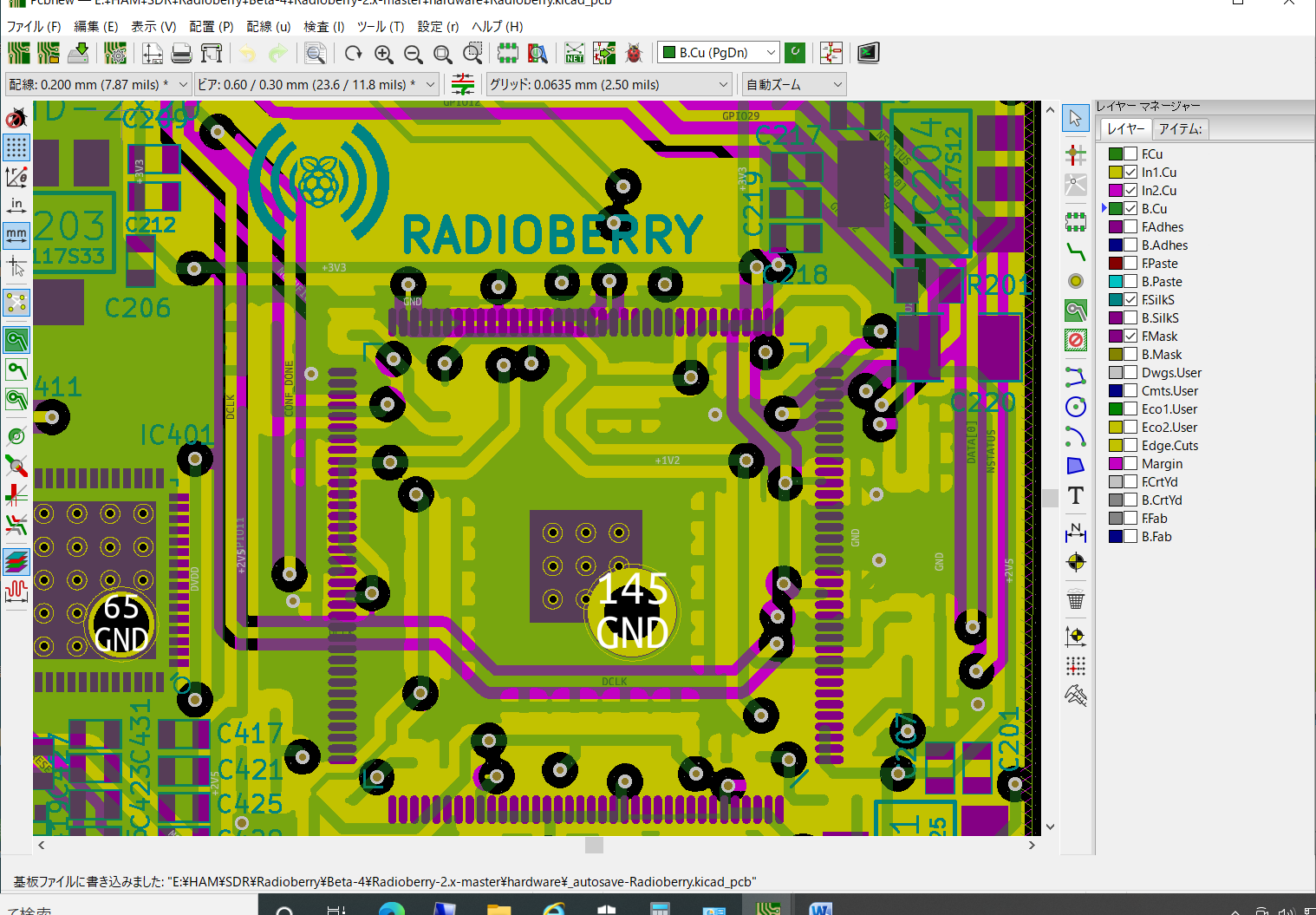
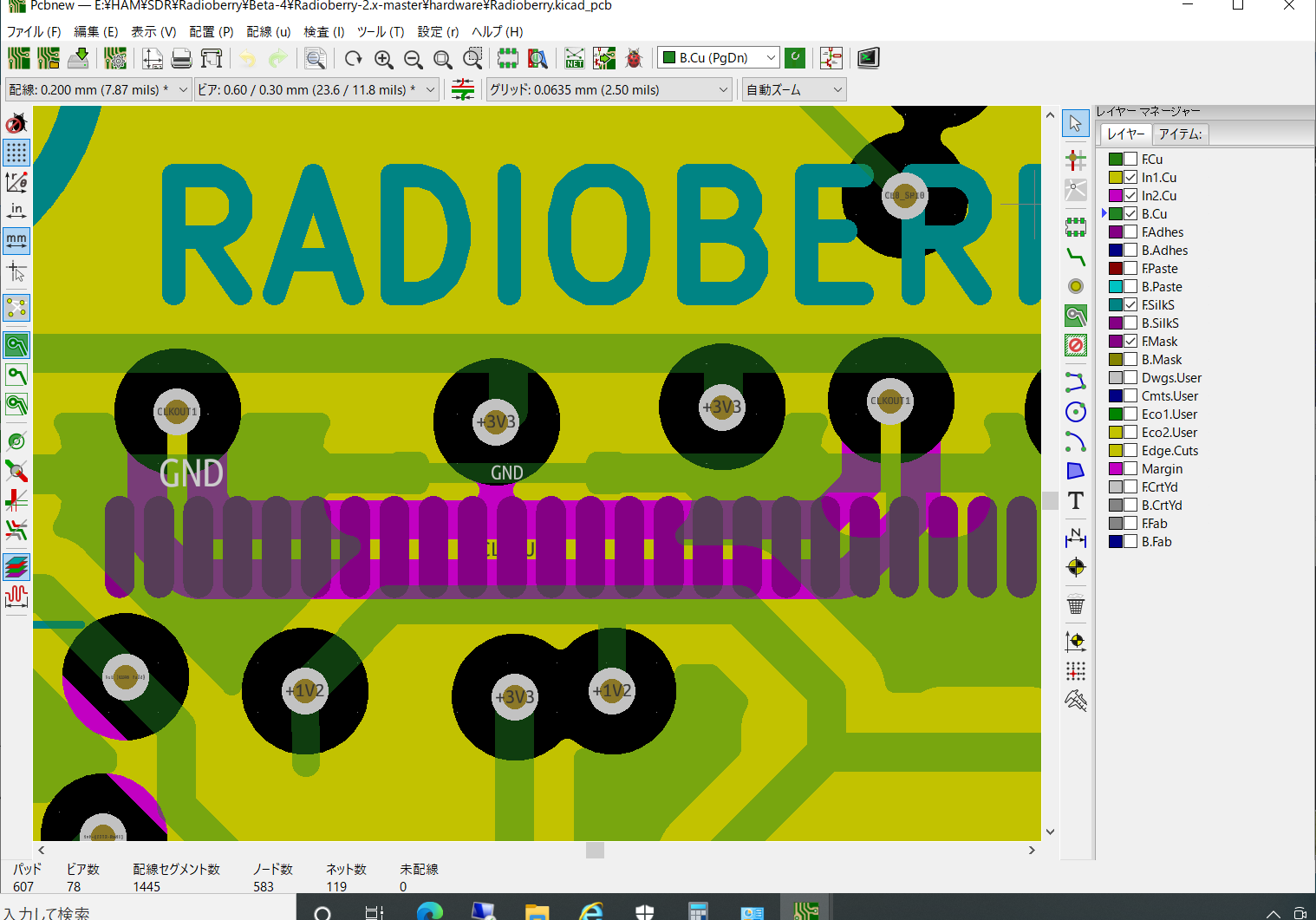
　　RB Beta4 PCB ADC/FPGA　　　　　　　FPGA 37pin

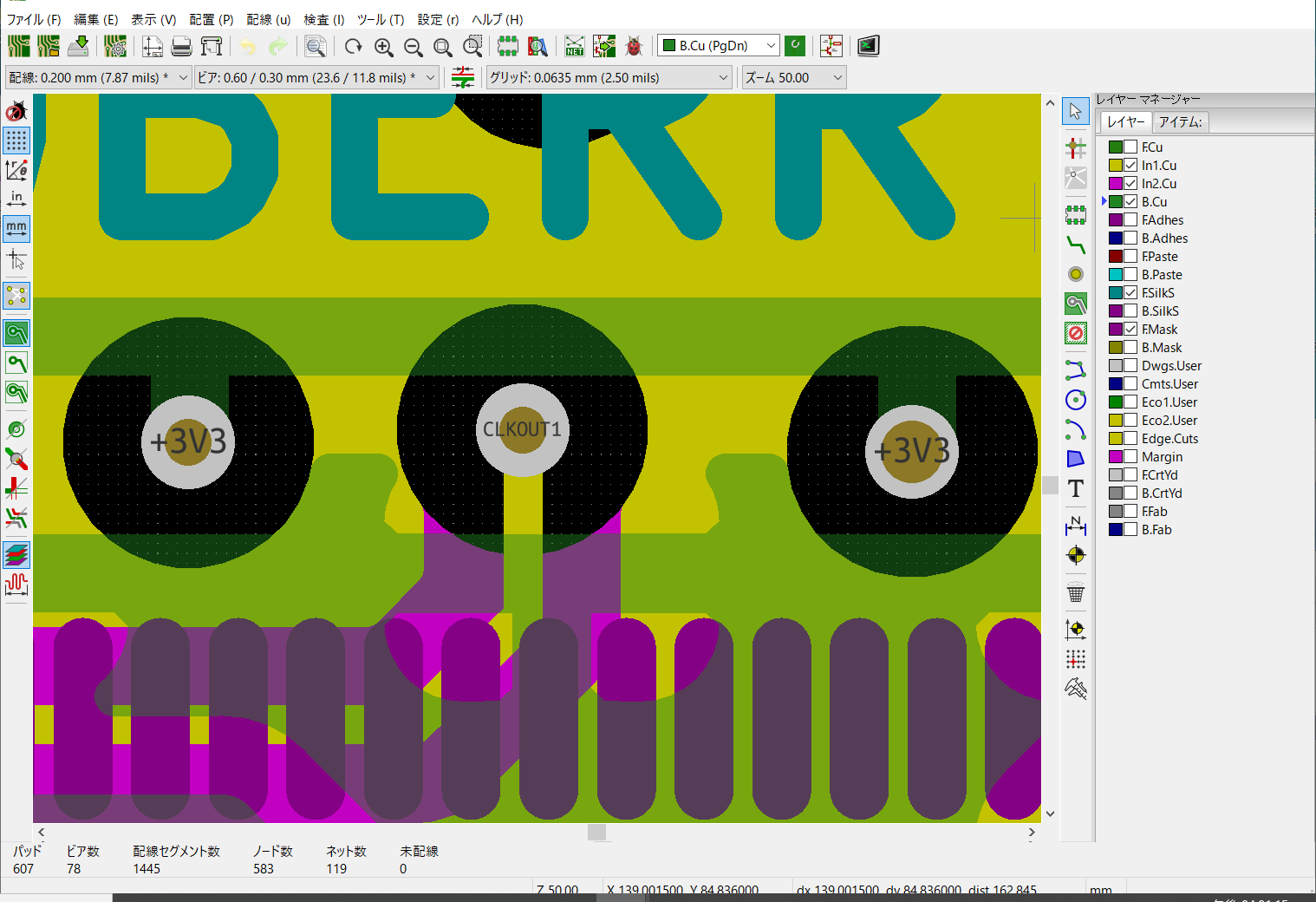


ADC FPGA 1pin

　　　69pin VIA 69-53pinconnection line(yellow)/Cu1 53pin VIA



53pin/Clockout1 VIA 🡨 🡪”3.3V line” spacing is about 2.5mil(=63.5μm)

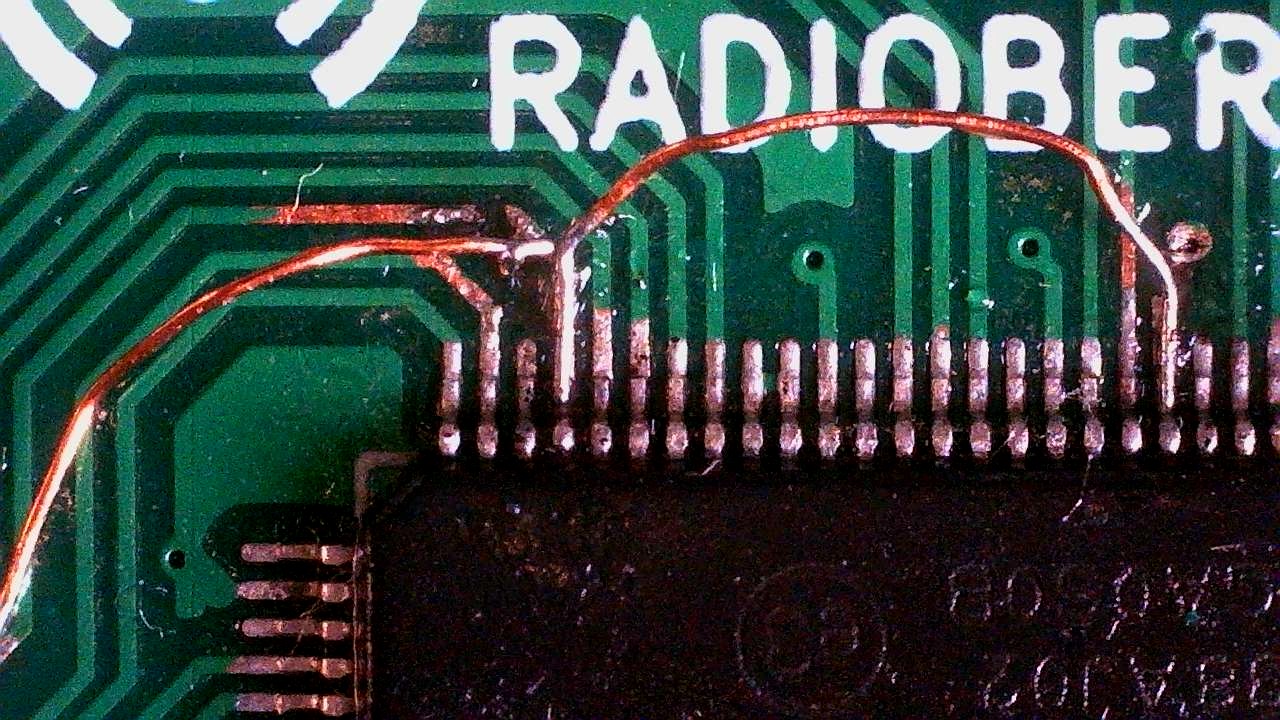


How to repair

1. Cut the lines between ADC Clock- Pin69 VIA, 69pin pad-pin69 VIA,

pin53 pad-pin53 VIA

1. wire ADC clock-69pin pad, 69pin pad-53pin pad



repaired