Universidad Nacional de San Luis

San Luis, 11 de noviembre de 2022

Estimado colega:

Debido a las numerosas solicitudes, se ha extendido el *deadline* para la presentación de trabajos a la **XI Southern Programmable Logic Conference SPL 2023.**

La realización de esta conferencia está organizada localmente por el Departamento de Electrónica de la **Facultad de Ciencias Físico Matemáticas y Naturales (FCFMyN) de la Universidad Nacional de San Luis (UNSL)**.

Nuevas fechas:

SPL Full Paper and Designer Forum Submission Deadline: December 5, 2022
Notification of acceptance date: December 29, 2022
Final Copy: February 15, 2023

Además, la organización otorgará **becas para los participantes nacionales.** Puede solicitarla a través del siguiente formulario:

https://forms.gle/LtEzRjz3vuoLRgEh7

Tarifas

	Antes de Feb 28, 2023 (early)		Después de Feb 28, 2023 (late)	
	Full	*Student*	*Full*	*Student*
Conferencia	ARS 15000	ARS 12000	ARS 18000	ARS 15000
Conferencia + workshops/tutorials	ARS 25000	ARS 20000	ARS 30000	ARS 22000
1 day workshops/tutorials	ARS 3200	ARS 2000	ARS 4800	ARS 3200
2 day workshops/tutorials	ARS 6400	ARS 4000	ARS 9600	ARS 6400
3 day workshops/tutorials	ARS 9600	ARS 6000	ARS 14400	ARS 9600
Presentación virtual	ARS 10000	ARS 8000	ARS 12500	ARS 10000

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La SPL Conference abarca un amplio espectro de temas relacionados con lógica programable incluyendo pero no limitada a:

- **Design Methodology and Tools**
- **Architectures and Technologies**
- **Applications and Benchmarks**
- **High-Level Abstractions**
- **High Performance, Acceleration, Data Processing**
- **Reconfigurable Computing and Adaptive Designs**
- **Hardware/software co-design**
- **Surveys, Trends, Education**

Workshops previos al congreso:

FPGA-based Accelerated Cloud Computing with AWS EC2 F1 and SDAccel

Tutorial Date: March 27, 2023
Presenters: Sergio Lopez-Buedo & Gustavo Sutter, Electratraining
Abstract: The evolution of reconfigurable computing in recent decades following Moore's law was impressive. Xilinx (now AMD) was the inventor of the FPGA back in the early 80s, later introduce Adaptable SoC (system on a chip) and recently the ACAP (Adaptive Computing Acceleration Platform) architecture. The evolution in terms of computing power is several orders of magnitude, leading to new tools and design methodologies, and also enabling new applications and uses of the technologies. This course reviews the key ideas in new devices and methodologies applied to embedded systems and cloud based HPC (High Performance Computing) platforms.

Developing Accelerators for AMD Xilinx adaptive computing platforms

Tutorial Date: March 28, 2023
Presenter: Xilinx
Abstract: This tutorial will introduce the Vitis Unified Software Platform environment for developing FPGA accelerators. Vitis environment enables the user to easily and productively develop accelerated algorithms and then efficiently implement and deploy them onto heterogeneous CPU-FPGA-ACAP systems. Vitis supports: C and C++ kernels. RTL design flows are also supported for experienced hardware developers. Each of these flows will be discussed along with the open-source Xilinx Runtime Library and Vitis open-source accelerated libraries. We will also introduce the PYNQ project and show how PYNQ makes the use of Xilinx accelerator much easier.

Para solicitud de información y envío de trabajos usar EasyChair:

email: spl23@easychair.org

Para más detalles visitar http://splconf.org.

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