Chip information

EC616S Data Sheet

EigenCOMM Wireless Microcontroller

Document description

This document describes the specifications of MobileCore's NB-IoT chip EC616S, SoC (system on chip), radio frequency, electrical Source management, pins, interfaces, electrical characteristics, packaging and other chip hardware information, for EC616S hardware engineers and software Software driver engineers provide references.

contents

1. Specification

EC616S is an ultra-low cost, ultra-low power consumption and ultra-high integration NB-IoT SoC chip developed by Shanghai Mobile Core Communication Technology Co., Ltd., It fully supports the 3GPP Rel14 NB-IoT standard.

EC616S has the following characteristics:

- Integrated RF transceiver, PA, RF filter, antenna switch and power management
- Excellent communication performance and stability in various wireless environments
- Excellent power consumption performance in various modes (PSM, DRX, eDRX, connected state)

- Unique MCU mode, providing lower working current and shorter wake-up time

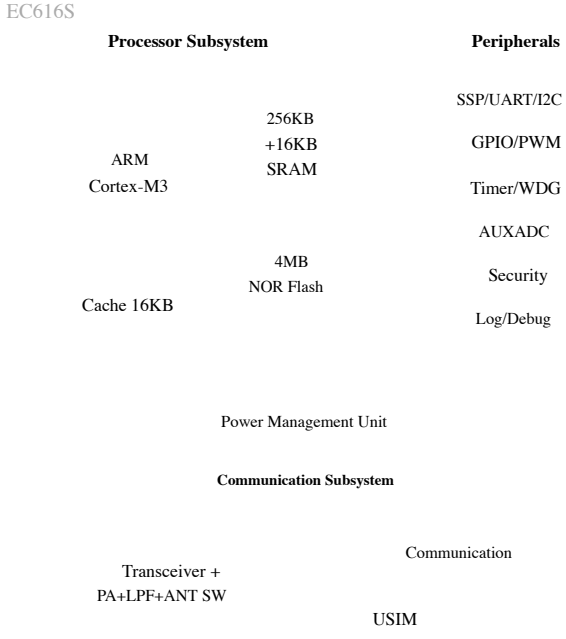


Figure 1-1: EC616S block diagram

1.1 characteristic

- Processor
  - Cortex-M3, support MPU
  - Configurable CPU frequency, up to 204MHz
  - 8-channel DMA
- Storage
  - 4MB on-chip NOR flash
  - 272KB on-wafer SRAM, divided into 256KB And 16KB two pieces
  - 16KB instruction cache
- System
  - Flexible configuration supports 1.8/2.8/3.3V IO
  - Clock source: 26MHz TCXO or DCXO, 32.768KHz crystal oscillator
  - 1 external wake-up source (interrupt)
  - Unique MCU mode, in which the internal RC oscillator as a clock, lower power consumption
  - LOG port, UNILOG
  - Debug port, SWD
- Peripherals
  - 16 GPIO
  - SC-PTM (need SW upgrade)
- Radio frequency
  - Support band: 1, 2, 3, 4, 5, 8, 18, 19, 20, 25, 26, 66, 70
  - Chip integrated PA, support APT function
  - Chip integrated radio frequency transceiver filter and antenna switch
  - Power level 3
- Security
  - Hardware encryption and decryption module (AES, SHA)
  - Secure boot
  - flash encryption
  - True random number generator
- Application
  - Support open-CPU
  - Software conforms to CMSIS architecture
  - Support mainstream cloud services
  - IPv4, IPv6 and non-IP
  - UDP, TCP
  - DTLS, TLS, SSL
  - MQTT, CoAP, HTTP(S)
  - LWM2M
  - Support FOTA
- Package

- 3 UART, 2 SSP, 2 I2C
- 6 PWM, 6 Timers, 6 GPIO counter, 1 WDG
- 32KHz RTC timer
- USIM, support Esim
- LPUART
- 4-channel 12-bit AUXADC
- Temperature Sensor
- Battery voltage monitoring

• Low power consumption
- Unique low-power architecture, 4-level sleep mode
- PSM: 800nA
- DRX (2.56s): 110uA typical
- RX: 10mA typical
- TX: 24mA typical

• Communication
- Fully support 3GPP R14 NB-IoT
- Category NB2, 2-HARQ
- Multi-tone NPUSCH
- Anchor and non-anchor carrier
- In-band same/different PCI, guard-band, standalone
- Multi-carrier paging, NPRACH
- Positioning: OTDOA & ECID
- ROHC, RAI, multiple-DRB, RRC connection re-establish

- 6mm*6mm*0.9mm QFN52, 0.4mm pitch

• Voltage range: 2.2V to 4.5V

2. SoC

2.1 Processor subsystem

The processor subsystem adopts a single-core architecture, that is, both the protocol software and application software run on a single CPU

- CPU adopts ARM Cortex-M3, supporting frequency 204M/102M/26M
- 8-entry MPU
- 8-channel DMA
- 16KB cache
- 256KB large SRAM and 16KB small SRAM, different low-power modes can maintain different SRAM content to achieve the lowest Sleep power consumption
- 4MB on-chip NOR flash
- Hardware encryption and decryption module
- Hardware log module, log output via UART and SSP
- 8 NVIC interrupt ports, two 32-port secondary interrupt controllers (XIC)

2.2 Communication subsystem

The communication subsystem includes the baseband hardware, radio frequency and protocol software of NB-IoT. The features are as follows:

- Fully support 3GPP R14 NB-IoT standard
- Support global frequency band
- Support Category NB2, maximum TBS = 2536
- Support 2-HARQ, combined with CAT-NB2, the data throughput rate is 5 times higher than that of CAT-NB1
- Support Multi-tone NPUSCH, support 1/3/6/12 sub-carrier
- Support Anchor and non-anchor carrier
- Support In-band same/different PCI, guard-band, standalone network deployment
- Support Multi-carrier paging and Multi-carrier NPRACH
- Positioning: OTDOA & ECID
- Others: ROHC, RAI, multiple-DRB, RRC connection re-establish
- Support SC-PTM (software upgrade required)

2.3 Peripheral Subsystem

Peripherals include:

- Maximum support 16 GPIO
- Support up to 6 GPIOs with input counting
- Support up to 3 UARTs
- Support up to 2 SSPs
- Support up to 2 I2C
- Maximum support 6 PWM, 6 Timer
- 1 WDG

- Support USIM and eSIM
- Support low power UART
- 4-channel 12-bit AUXADC
- Temperature Sensor
- Battery voltage monitoring

2.4 Clock subsystem

EC616S needs two external clock sources, 26M crystal and 32.768K crystal. Among them, 26M crystal provides clock for radio frequency and SoC, 32.768K provides the clock source for the power management module (PMU) and also provides the clock for the timer in the SoC. As shown below:

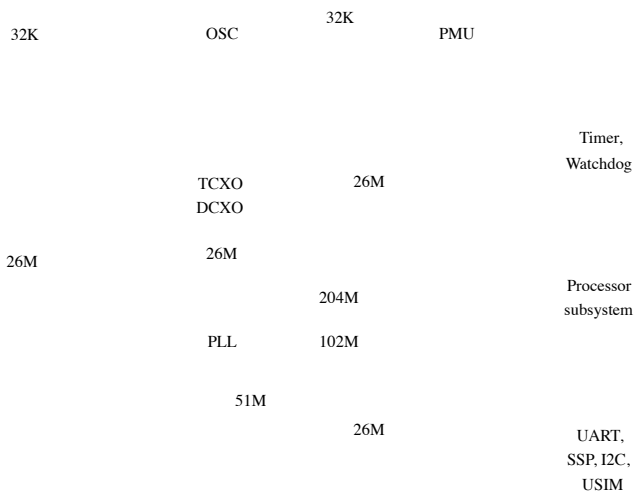


Figure 2.4-1: EC616S clock subsystem

3. Radio frequency

3.1 RF system block diagram

The radio frequency system is shown in the figure below:

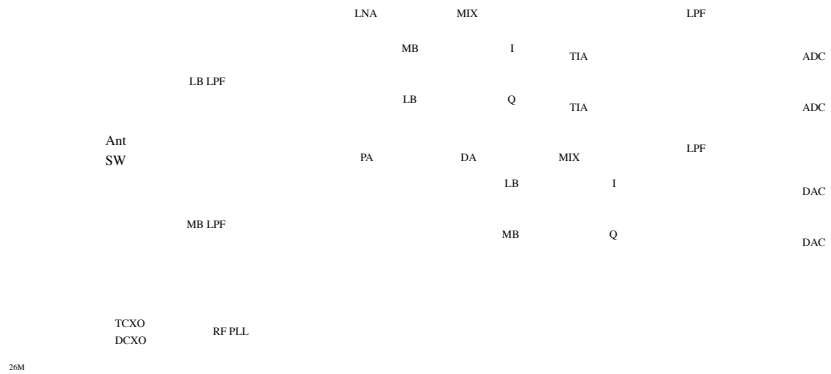


Figure 3.1-1: EC616S RF system

3.2 Frequency band

The frequency bands supported by EC616S are divided into low frequency bands and high frequency bands, as shown in Table 3.2-1:

Table 3.2-1: EC616S support frequency band

Frequency band classification	Frequency Range	Band number
Low frequency band	698MHz – 960MHz	5, 8, 12, 13, 14, 17, 18, 19, 20, 26, 28, 85
High frequency band	1695MHz – 2200MHz	1, 2, 3, 4, 25, 66, 70

4. Power management

4.1 voltage

The main power supply voltage in the chip is shown in Table 4.1-1:

Table 4.1-1: EC616S power supply

power supply	Typical voltage	Power supply object
SIMO11DIG	1.1V	number
SIMO19FLASH	1.9V	FLASH, TCXO
SIMO15RF	1.5V	Radio frequency
DCDCPA	APT adjustable	RF PA
LDO_SIM	1.8/3.0V	SIM card
LDO_1833IO	1.8V/2.8/3.3V	I/O interface

4.2 Power configuration

According to the needs of peripheral devices and circuits, the configurable power supply and voltage are shown in Table 4.2-1:

Table 4.2-1: EC616S configurable power supply

Configurable voltage	Chip internal power supply	Voltage value
GPIO and peripheral interface voltage	LDO_IO	1.8V/2.8V/3.3V optional
USIM supply voltage	LDO_SIM	1.8V/3.0V optional

4.3 Power state

EC616S supports the following power consumption states:

Table 4.3-1: EC616S power consumption in different states

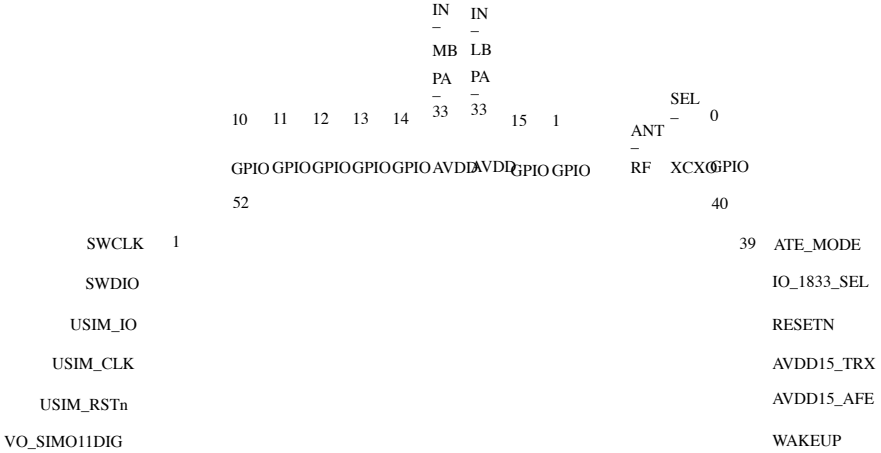
Power state name	application	Current
Running state	CPU is running	From top to bottom, Decreasing current
Idle state	The CPU is in WFI (IDLE), and the main body is not powered down	
Sleep state 1	The main body is powered off, 16KB SRAM retains the content, 256KB SRAM retains the content	
Sleep state 2	The main body is powered off, 16KB SRAM retains the content, 256KB SRAM does not retain the content	

Sleep state 1	The main body is powered off, and the SRAM does not retain the content
Sleep state 2	The main body is powered off, and the SRAM does not retain the content

5. Pin

5.1 Pin mapping

EC616S is a 6mm*6mm QFN52 package, 0.4mm pitch, the top view of the pin definition is shown in Figure 5.1-1



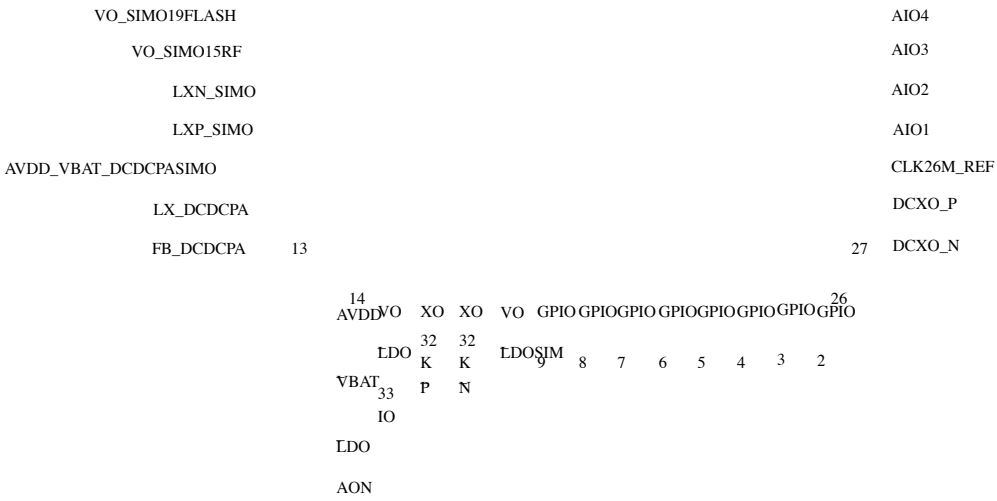


Figure 5.1-1. EC616S ball diagram, top view

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5.1.1 Pin definition

Table 5.1.1-1 Pin definition

Pin#	NETNAME	Pin#	NETNAME
1	SWCLK	27	DCXO_N
2	SWDIO	28	DCXO_P
3	USIM_IO	29	CLK26M_REF
4	USIM_CLK	30	AIO1
5	USIM_RSTn	31	AIO2
6	VO_SIMO11DIG	32	AIO3
7	VO_SIMO19FLASH	33	AIO4
8	VO_SIMO15RF	34	WAKEUP
9	LXN_SIMO	35	AVDD15_AFE
10	LXP_SIMO	36	AVDD15_TRX
11	AVDD_VBAT_DCDCPASIMO	37	RESETN
12	LX_DCDCPA	38	IO_1833_SEL
13	FB_DCDCPA	39	ATE_MODE
14	AVDD_VBAT_LDOAON	40	GPIO0
15	VO_LDO33IO	41	XCXO_SEL
16	XO32K_P	42	RF_ANT
17	XO32K_N	43	NC
18	VO_LDOSIM	44	GPIO1
19	GPIO9	45	GPIO15
20	GPIO8	46	AVDD33_PALB_IN
twenty one	GPIO7	47	AVDD33_PAMB_IN
twenty two	GPIO6	48	GPIO14
twenty three	GPIO5	49	GPIO13
twenty four	GPIO4	50	GPIO12
25	GPIO3	51	GPIO11
26	GPIO2	52	GPIO10

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5.1.2 Pin description

Pin Number	Pin Name	Pin Type	Power Domain	Pin Description
PIN39	ATEMODE	AI	VDD12AON	Auto-Test-Equipment Test Mode Should be left unconnected or tied to ground
PIN37	RESETn	AI	VDD12AON	System Reset Active-low, Assertion of RESETn causes EC616 entering power-up sequence and whole chip will go to reset state.
PIN38	IO_1833_SEL	AI	VDD12AON	IO Voltage selection Floating: 1.8V 0: 3.3V
PIN41	XCXO_SEL	AI	VDD12AON	Clock selection-on chip DCXO or external clock 0: DCXO 1: TCXO
PIN34	WAKEUP	AI	VDD12AON	External Wakeup Source
PIN16	XTAL32KP	AI	VDD12AON	Input pin for 32k crystal
PIN17	XTAL32KN	AI	VDD12AON	Input pin for 32k crystal
PIN3	USIM_UIO	DIO	VDDSIM	SIM card IO
PIN4	USIM_UCLK	DIO	VDDSIM	SIM card clock
PIN5	USIM_URSTn	DIO	VDDSIM	SIM card reset
PIN1	SWCLK	DIO	VDDIO	Serial Wire Debug Clock
PIN2	SWDIO	DIO	VDDIO	Serial Wire Debug Data
PIN40	GPIO0	DIO	VDDIO	General Purpose I/O
PIN44	GPIO1 (boot flag)	DIO	VDDIO	General Purpose I/O
PIN 26	GPIO2	DIO	VDDIO	General Purpose I/O
PIN25	GPIO3	DIO	VDDIO	General Purpose I/O
PIN24	GPIO4	DIO	VDDIO	General Purpose I/O
PIN23	GPIO5	DIO	VDDIO	General Purpose I/O
PIN22	GPIO6	DIO	VDDIO	General Purpose I/O
PIN21	GPIO7	DIO	VDDIO	General Purpose I/O
PIN20	GPIO8	DIO	VDDIO	General Purpose I/O
PIN19	GPIO9	DIO	VDDIO	General Purpose I/O
PIN52	GPIO10	DIO	VDDIO	General Purpose I/O
PIN51	GPIO11	DIO	VDDIO	General Purpose I/O
PIN50	GPIO12	DIO	VDDIO	General Purpose I/O

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PIN 49	GPIO13	DIO	VDDIO	General Purpose I/O
PIN48	GPIO14	DIO	VDDIO	General Purpose I/O
PIN45	GPIO15	DIO	VDDIO	General Purpose I/O
PIN30	AIO1	AIO	AVDDIO	ADC Channel
PIN31	AIO2	AIO	AVDDIO	ADC Channel
PIN32	AIO3	AIO	AVDDIO	ADC Channel
PIN33	AIO4	AIO	AVDDIO	ADC Channel
PIN35	AVDD15_AFE	PI		AFE supply 1.5V
PIN36	AVDD15_TRX	PI		TRX supply 1.5V
PIN46	AVDD33_PALB_IN	PI		LB PA supply
PIN47	AVDD33_PAMB_IN	PI		MB PA supply
PIN28	DCXO_P	AI	AVDD_DCXO	26MHz crystal input, 26MHz TCXO input
PIN27	DCXO_N	AI	AVDD_DCXO	26MHz crystal input
PIN29	CLK26M_REF	AO	AVDD_DCXO	26MHz REF Clock output
PIN42	RF_ANT	AI	AVDD15LNA	RF input for LB
PIN11	AVDD_VBAT_DCDCPASIMO	PI		VBAT for DCDC
PIN14	AVDD_VBAT_LDOAON	PI		VBAT for AON and LDO
PIN6	VO_SIMO11DIG	PI		SIMO output for Digital, 1.1V
PIN7	VO_SIMO19FLASH	PO		SIMO output for Flash, 1.9V
PIN8	VO_SIMO15RF	PI		SIMO output for RF, 1.5V
PIN9	LXN_SIMO	PO		
PIN10	LXP_SIMO	PI		
PIN12	LX_DCDCPA	PO		SW node of DCDC_PA
PIN13	FB_DCDCPA	PI		Feedback of DCDC_PA
PIN15	VO_LDO_1833IO	PO		Output of LDO_1833IO, 1.8V/2.8V/3.3V
PIN18	VO_LDOSIM	PO		Output of LDO_SIM, 1,8V/3.0V

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5.2 Pin multiplexing

Table 5.2-1: Pin function description

I/O	Pad Name	Cfg Offset	Powerup Default	Alt Func0	Alt Func1	Alt Func2	Alt Func3	Alt Func4	Alt Func5	Alt Func6	Alt Func7
USIM	USIM_UIO	0	IO, NP	USIM_UIO					PWM1		
	USIM_URSTn	1	O, NP	USIM_URSTn					PWM2		
	USIM_UCLK	2	O, NP	USIM_UCLK					PWM3		
SWD	SWCLK	9	I, PU	SWCLK	UART1_RTSn	I2C1_SDA	UART2_RXD		PWM4		
	SWDIO	10	I, PU	SWDIO	UART1_CTSn	I2C1_SCL	UART2_TXD		PWM5		
GPIO	GPIO0	11	I, PU	GPIO0							
	GPIO1	12	I, PU	GPIO1							
	GPIO2	13	I, PU	GPIO2		I2C0_SDA		SPI0_SSn1	PWM0		
	GPIO3	14	I, PU	GPIO3		I2C0_SCL		SPI0_SSn0	PWM1		
	GPIO4	15	I, PU	GPIO4		I2C1_SDA	UART2_RXD	SPI0_MOSI	PWM2		
	GPIO5	16	I, PU	GPIO5		I2C1_SCL	UART2_TXD	SPI0_MISO	PWM3		
	GPIO6	17	I, PU	GPIO6	UART0_RTSn	I2C0_SDA		SPI0_SCLK	PWM4		
	GPIO7	18	I, PU	GPIO7	UART0_CTSn	I2C0_SCL			PWM5		
	GPIO8	19	I, PU	GPIO8	UART0_RXD				PWM0		
	GPIO9	20	I, PU	GPIO9	UART0_TXD				PWM1		
	GPIO10	twenty one	I, PU	GPIO10	UART1_RTSn	I2C1_SDA		SPI1_SCLK	PWM2		
	GPIO11	twenty two	I, PU	GPIO11	UART1_CTSn	I2C1_SCL		SPI1_MOSI	PWM3		
	GPIO12	twenty three	I, PU	GPIO12	UART1_RXD	I2C0_SDA	UART2_RXD	SPI1_MISO	PWM4		
	GPIO13	twenty four	I, PU	GPIO13	UART1_TXD	I2C0_SCL	UART2_TXD	SPI1_SSn0	PWM5		
	GPIO14	25	I, PU	GPIO14	UART1_RXD			SPI1_SSn1	PWM0		
	GPIO15	26	I, PU	GPIO15	UART1_TXD				PWM1		

IO: Input/output

I : Input

O : Output

NP: No pull up/down

PU: Pull up

PD: Pull down

6. interface

6.1 UART

Up to 3 UARTs can be configured

- Configurable baud rate, 4.9Kbps, 9.6Kbps, 115.2Kbps, 921.6Kbps, up to 3MBps
- Independent 32Bytes TX/RX FIFO
- Support sending and receiving 5~8 bit data length characters
- Support odd parity, even parity and no parity
- Support 1 or 2 bit stop bit

- Support DMA operation
- Support flow control (UART0/1)
- Support NRZ encoding

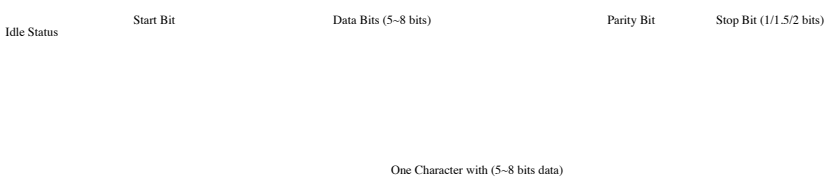

Figure 6.1-1: UART interface timing diagram

6.2 LPUART

UART1 of the above 3 UARTs can be configured as LPUART when using GPIO14&GPIO15 as RXD/TXD

- Continuously receive AT commands in low power consumption mode
- Configurable baud rate, 9.6Kbps, 4.8Kbps, 2.4Kbps,…
- Independent 32Bytes TX FIFO, 72Bytes RX FIFO
- Support sending and receiving 5~8 bit data length characters
- Support odd parity, even parity and no parity
- Support 1 or 2 bit stop bit
- Support DMA operation
- Support frame structure and check bit error and timeout detection
- Support switching to ordinary UART to achieve higher baud rate

6.3 I2C

Up to 2 I2C can be configured

- Configurable clock up to 400KHz
- Can be configured as Master or Slave
- Independent 16Bytes TX/RX FIFO
- Support 7/10bit address
- Support DMA operation
- Support clock extension
- Configurable SCL waveform

6.4 SPI

Up to 2 SPIs can be configured

- Configurable clock up to 25.6MHz
- Can be configured as Master or Slave
- Independent TX/RX FIFO
- Configurable CPOL/CPHA
- Support DMA operation

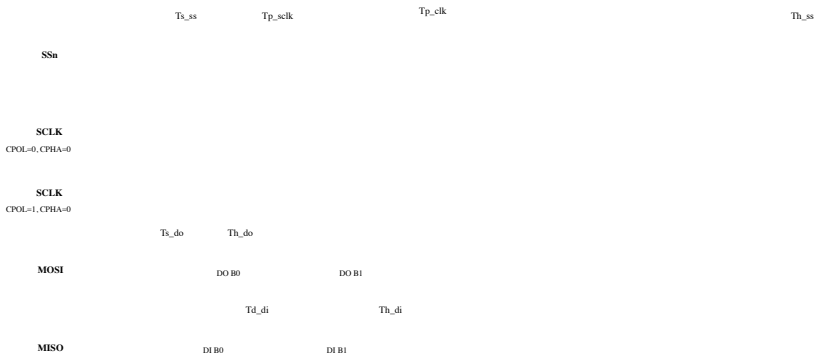

Figure 6.4-1: SPI master interface timing diagram CPHA=0

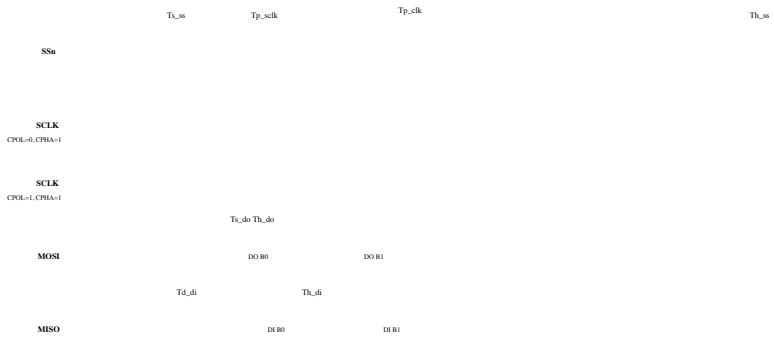

Figure 6.4-2: SPI master interface timing diagram CPHA=1

Table 6.4-1: SPI master interface parameters

Signal	Symbol	Min	Max	Unit	Description
SCLK	Tp_sclk	38.4		ns	
SSn	Ts_ss	9.6		ns	
	Th_ss	2.0		ns	
MOSI	Ts_do	9.6		ns	
	Th_do	twenty one		ns	
MISO	Td_di		Tp_sclk/2-12	ns	

6.5 AUXADC

6.5.1 **AUXADC** block diagram

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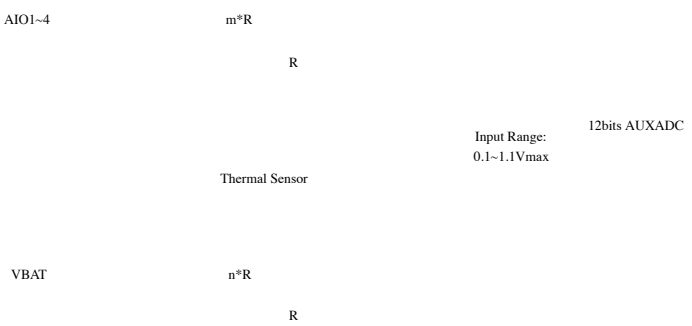

Figure 6.5-1: AUXADC block diagram

AUXADC includes the following functional modules:

(1) Analog channel selection module: select one of AIO1~4 as the analog signal path, after adjusting the voltage divider circuit, send the voltage signal Enter the input port of AUXADC.

(2) Temperature sensor: When the chip temperature changes, the voltage output signal of the Thermal Sensor also changes.

(3) 12-bit AUXADC: quantize the input voltage signal into 12-bit digital data.

Table 6.5-1: AUXADC input channel

Channel	**Application**	**Input Range**
AIO1	Input signal from the outside	0V ~ 1.8V
AIO2~4	Input signal from the outside	0V ~ 3.3V
Thermal Sensor	Inner thermal sensor generate the signal	-40°C ~ 85°C
VBAT	VBAT voltage input	2.2V ~ 4.5V

6.5.2 Functional Specifications

Parameter setting:

When the external input voltage of any one of AIO2~4 can fluctuate in the range of 0~3.3V, but the voltage divider ratio needs to be adjusted, make sure that AUXADC The input voltage is in the range of 0.1~1.1V.

Table 6.5-2: AUXADC technical parameters

Symbol	**Description**	**Min.**	**Typ.**	**Max**	**Unit**
N	Resolution	-	12	-	Bit
Fc	Clock rate	1.625	3.25	6.5	MHz
Fs	Sampling rate	-	Fc/(N+4)	-	MHz
Vin	Input swing	0.1	-	1.1	V

Cin	Input capacitance:				
	-Unselected channel	-	0.1	-	pF
	-Selected channel	-	1.2	-	pF
Rin	Input resistance:				
	-Unselected channel	29	-	-	MΩ
	-Selected channel	0.26	-	0.75	MΩ
DNL	Differential nonlinearity	-	±1	-	LSB
INL	Integral nonlinearity	-	±4	-	LSB
DVDD	Digital power supply	0.99	1.1	1.21	V
AVDD	Analog power supply	2.00	2.1	2.21	V
Temp	Operating temperature	-40	-	85	°C
	Current consumption:				
	-Power up	-	300	-	uA
	-Power down	-	0.4	-	uA

7. Encapsulation

7.1 Package mechanical size

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Figure 7.1-1: EC616S package dimensions

7.2 Chip screen printing

Line0: Mobile Core Communication Logo

Line1: chip name + internal control number

Line3: Wafer lot number

Line4: Assembly batch number

Line5: Internal control number + internal control number + year and week number

Figure 7.2-1: EC616S mass production top logo

7.3 Reflow soldering

Reflow soldering is performed in accordance with IPC/JEDEC J-STD-020. The maximum allowable number of reflow soldering is 3 times.

7.4 Environmental friendly

Meet RoHS 2.0 and halogen-free standards.

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8. Version

Version	date	Remark
Draft	2019-12-11	
A	2019-12-01	